# Analysis and Design of Low Power Ring Oscillators with Frequency ~10-100 kHz



**PRESENTED BY:**

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# Certificate

*Certified that this project report titled*

## "Analysis & Design Of Low Power Ring Oscillators with Frequency ~10-100 kHz "

*By*

## Piyush Keshri

is approved by us for submission. Certified further that the report represents the work carried out by the student in Computer Science Dept. Lab under our guidance and support during May – July '2008.

**Date:** **Prof. David Blaauw** **Prof. Dennis Sylvester**

# Abstract

In the Era of digital World, low power applications are the needs of the market to save the resources. Delay elements (e.g. digital clock) are essential parts of such digital applications. Hence, generation of such low power clocks is a major issue of research.

Precise clock generation independent of supply and temperature sensitivity has been the main objective in various applications such as DC-DC converters. Precise delay can be generated using ring oscillators by using the symmetry of the oscillator ring.

Ring oscillators have been used because of their ease of implementation, wide tuning ranges, operating at low voltages and existing possibility of complete integration in standard CMOS processes. They also occupy smaller chip area.

This project has been aimed at designing a clock with low power, low frequency, and low operating voltage using ring oscillator topology. It aims at determining the best possible configuration for the ring oscillators having the least power consumption and precise delay with lesser sensitivity to the variations in the temperature and supply voltage for frequencies of few kHz. The oscillator configurations have been designed at frequencies of 10 kHz and 100 kHz for an IBM 0.13µm and ST 65nm CMOS processes each.

The design of clock using ring oscillator of a wide range, low sensitivity to the variations of the supply, but mainly low power consumption has been detailed in this work. The various topologies of ring oscillators like simple Vt Inverter Chain, stacked Inverter Chain, Current Starved, High Vt transistors, CMOS Thyristor and CMOS Thyristor with footer have been explored in this project, to determine the sensitivities of each topology w.r.t variations in the temperature and supply. Monte Carlo analysis has been performed to determine the effect of Process Mismatch over the performance of the oscillator. Efforts have been put in to determine an optimum frequency for each topology to minimize the power consumption and maximise the efficiency (determining the 'sweet point').

Problems faced during the project regarding the design and improving performance have been mentioned in the text and few suggestions/solutions/future prospects for the future research have been tried to describe in the project. New ideas for a different kind of topology with lesser power, lesser sensitivity with variations in the environment parameters like temperature & voltage needs to be introduced and some cool ideas has also been tried to implement.

It still remains an open problem to come up with a better circuit with better performance and to determine optimum performance criterion for each topology. The research over such problem still continues and will form the next level for this project.

# Table of Contents

# Chapter 1 Background of Ring Oscillator & its various Configurations

## 1.1 Definition

The ring oscillators consist of odd number of inverters used as delay cells connected in cascade and in a closed loop, which provide enough gain and phase shift to satisfy the Barkhausen's oscillation criteria.

In these topologies the oscillation frequency is given by:

$$f = \frac{1}{2N\tau_d}$$

Where, N is the number of delay cells in the ring and $\tau_d$ is the delay time in the cell.

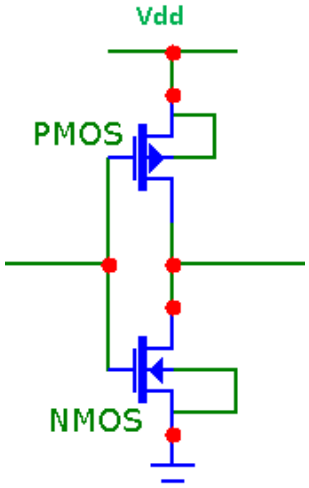



**Fig. 1(a)** CMOS Inverter

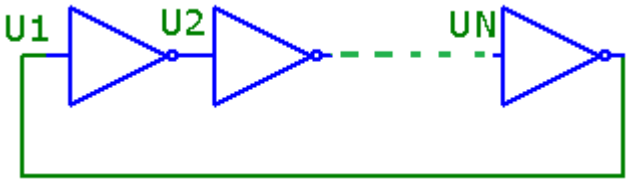



**Fig. 1(b)** Inverter Chain to form Ring Oscillator

## 1.3 Different Configurations of Ring Oscillators

1.3.2 Minimum Sized SVT (Simple Vt) Transistor Inverter Chain
1.3.3 SVT (Simple Vt) Transistors Inverter Chain
1.3.4 Double Stacked SVT Inverter Chain
1.3.5 HVT (High Vt) Transistors Inverter Chain
1.3.6 Current Starved Inverter Chain
1.3.7 CMOS Thyristor Inverter Chain
1.3.8 CMOS Thyristor with Footer Inverter Chain

### 1.2.1 Minimum Sized SVT (Simple Vt) Transistor Inverter Chain

Inverters consist of Simple Vt transistors of minimum sized i.e. length and width of transistor is minimum, cascaded in an inverter chain. The number of transistors has been determined by fixing the frequency of oscillations for desired frequency.

### 1.2.2 SVT (Simple Vt) Transistors Inverter Chain

In this case the inverters consist of simple vt transistors with the length and width of each transistor sized to get the desired frequency with the minimum power

consumption. The number of transistors has been determined by minimising the power consumed for a particular frequency with different no. of transistors in the inverter chain.

### 1.2.3 Double Stacked SVT Inverter Chain

Simple vt transistors are double stacked so that the source and drain terminals of NMOS & PMOS transistors respectively are floating ground and floating Vdd.

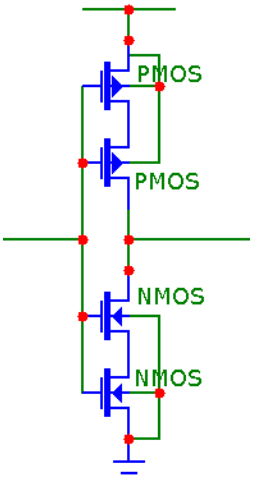



**Fig.** Circuit Diagram of Double Stacked Inverter

### 1.2.4 HVT (High Vt) Transistors Inverter Chain

High Vt MOSFETs are used rather than Simple Vt. Thses high vt transistors have higher Vt values.The circuit design is same as that of SVT inverter chain.

### 1.2.5 Current Starved Inverter Chain

Starving is done using biasing circuit which the delay of each cell depending upon the extent of starving based on the biasing voltage and the scaling of the MOSFETs. It also improves the efficiency of the system by reducing the power consumption.

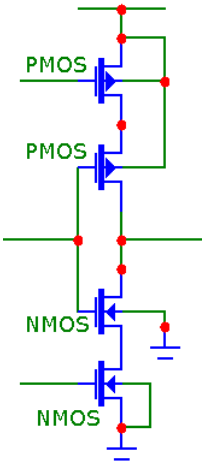



**Fig.** Inverting Delay cell of Current Starved Oscillator.

### 1.2.6 CMOS Thyristor Inverter Chain

CMOS Thyristor design has been proposed recently, which is considered to be less sensitive to conditions like voltage as it depends on leakage current and not on voltage of operation.

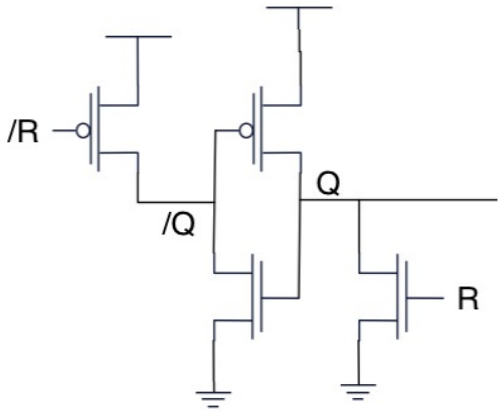



**Fig.** Circuit Diagram of each Inverting Delay Cell in CMOS Thyristor Design

### 1.2.7 CMOS Thyristor with Footer

It uses header and footer to provide floating Vdd & ground to the invertering MOSFETs to reduce power consumption further by increasing the delay of the cell.

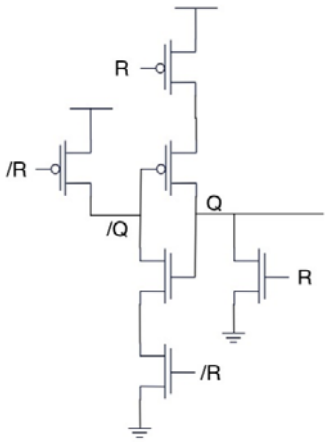



**Fig.** Circuit Diagram of a Delay Cell in the CMOS Thyristor with Footer design.

# Chapter 2 Analysis of various Topologies in IBM 130nm Technology

## 2.1 Power Consumption for frequency of 100 kHz for various configurations

In this section, optimum value of power consumption for each configuration is determined by scaling the transistors (exception is the minimum sized Inverter Chain) and changing the number of inverters for the fixed frequency of oscillator at 100 kHz.

The Length of the transistors are kept below 50um so that fabrication is easier. The width of the transistors is small to reduce the current (by reducing W/L ratio) and thus, increasing the delay of each cell and hence, reducing the overall frequency of oscillation of the ring oscillator.

**NOTE:** Wmin = 160 nm
Lmin = 120 nm
Vpp – peak-to-peak voltage of the oscillations

### 2.1.1 Supply Voltage, Vdd=1.2Volts

| Type | No. Of Inverters | W | L | Power (nW) | Frequency (kHz) |
|---|---|---|---|---|---|
| Min. size Inverter Chain | ------- | ------- | ------- | -------- | ------- |
| SVT Inverter Chain | 7 | Wmin | 46.95u | 184.76 | 100 |
| HVT Inverter Chain | 5 | Wmin | 41.34u | 79.6 | 100 |
| Stack Inverter Chain | 3 | Wmin | 41.86u | 98.86 | 100 |
| Current Starved $V_b$=0.1v | 3 | 240n Wmin | 220n 13.5u | 10.92 | $V_{pp}$ (0.15-1.082V) |
| CMOS Thyristor | 3 | Wmin 200n | 4.1u 3.3u | 23.92 | 100 |
| CMOS Thyristor Footer | 3 | 180n 400n | 4.69u 120n | 8.947 | 100 |

**Table 2.1 Optimised Table for Minimum Power Consumption by diff. Topologies for 100 kHz at 1.2 volts.**

### 2.1.2 Supply Voltage, Vdd =0.9Volts

| Type | No. Of Inverters | W | L | Power (in nW) | Frequency |
|---|---|---|---|---|---|
| Min. size Inverter Chain | ----- | ------- | ------ | ------- | -------- |

| | | | | | |
|---|---|---|---|---|---|
| SVT Inverter Chain | 5 | Wmin | 47.34u | 68.56 | 100 |
| HVT Inverter Chain | 3 | Wmin | 41.8u | 22.7 | 100 |
| Stack Inverter Chain | 3 | Wmin | 34.15u | 44.22 | 100 |

**Table 2.2 Optimised Table for Minimum Power Consumption by diff. Topologies for 100 kHz at 0.9 volts.**

### 2.1.3 Supply Voltage, Vdd =0.6Volts

| Type | | No. Of Inverters | W | | L | | Power ( nW) | Frequency |
|---|---|---|---|---|---|---|---|---|
| Min. size Inverter Chain | | 18k+1 | Wmin | | Lmin | | $1.72 \times 10^{3}$ | 680 |
| | | 27k+1 | | | | | ----- | 130.72 |
| SVT Inverter Chain | | 3 | Wmin | | 47u | | 13.92 | 100 |
| HVT Inverter Chain | | 3 | 265n | | 17.11u | | 4.738 | 100 |
| Stack Inverter Chain | | 3 | Wmin | | 23.86u | | 13.26 | 100 |
| Current Starved | $V_b$=0.1v | 3 | 241n | Wmin | 0.69u | 0.12u | 2.805 | $\mathbf{V_{pp}}$ (0.20-0.515V) |
| CMOS Thyristor | | 3 | Wmin | | 3u | 3.86u | 4.364 | 100 |
| CMOS Thyristor Footer | | 3 | 246n | 200n | 0.77u | 120n | 1.765 | 100 |

**Table 2.3 Optimised Table for Minimum Power Consumption by diff. Topologies for 100 kHz at 0.6 volts.**

### 2.1.4 Supply Voltage, Vdd =0.3Volts

| Type | | No. Of Inverters | W | | L | | Power (in nW) | Frequency(kHz) |
|---|---|---|---|---|---|---|---|---|
| Min. size Inverter Chain | | 935 | Wmin | | Lmin | | 20.02 | 100 |
| SVT Inverter Chain | | 3 | Wmin | | 18.76u | | 1.13 | 100 |
| HVT Inverter Chain | | 3 | 265n | | 147.5n | | $37.67 \times 10^{-3}$ | 100 |
| Stack Inverter Chain | | 3 | Wmin | | 9.35u | | 1.06 | 100 |
| Current | $V_b$=0.1v | 3 | 240n | 160n | 3.83u | 17u | $917 \times 10^{-3}$ | $\mathbf{V_{pp}}$ |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Starved | | | | | | | | (19-186.4mV) |
| CMOS Thyristor | | 3 | 160n | | 4.09u | 3.1u | 927.9 x $10^{-3}$ | 100 |
| CMOS Thyristor Footer | | 3 | 280n | 160n | 316n | 120n | 409.9 x $10^{-3}$ | 100 |

**Table 2.4 Optimised Table for Minimum Power Consumption by diff. Topologies for 100 kHz at 0.3 volts.**

## 2.2 Monte Carlo Results for the configurations

Monte Carlo simulations over the whole project have been performed with,
**No. of Iterations, # = 1000**
At voltages**, Vdd = 0.3 volts/ 0.6 volts/ 1.2 volts**
over all the topologies, to determine the effect of "**Process & Mismatch**" over the performance of the ring oscillator.

### 2.2.1 Monte Carlo analysis at voltages 0.3 volts, 0.6 volts & 1.2 volts respectively

| Type | | Voltage, V=1.2 volts | | Voltage, V=0.6 volts | | Voltage, V=0.3 volts | |
|---|---|---|---|---|---|---|---|
| | | Mean, mu | Standard Deviation, sd (in kHz) | Mean, mu (in kHz) | Standard Deviation, sd (in kHz) | Mean, mu (in kHz) | Standard Deviation, sd (in kHz) |
| Minimum sized Inverter Chain (5) | | | | | | 97.0716 | 14.41 |
| SVT W-L Optimised | | 96.4122 | **4.59516** | 94.8019 | **6.82339** | 94.7357 | 17.4762 |
| HVT Inverter | | 98.6651 | 14.4358 | 97.3167 | 23.8747 | 110.687 | 92.7469 |
| Stacked Inverter | | 99.1446 | 5.23474 | 92.2865 | 6.90043 | 92.3989 | **17.0309** |
| Current Starved | $V_b$=0.1v | 121.555 | 56.7641 | 107.81 | 48.9161 | 91.4288 | 42.7021 |
| CMOS Thyristor | | 106.807 | 37.6986 | 115.141 | 43.1907 | 107.439 | 39.5774 |
| CMOS Thyristor Footer | | 110.867 | 57.6057 | 110.221 | 68.3668 | 114.369 | 77.6809 |

**Table 2.5 Table for Monte Carlo Analysis for diff. Topologies at 100 kHz for diff. Vdd.**

The Monte Results shows that the Simple Vt (SVT) has the smallest values of σ (sd). Hence, it is least sensitive to the Process mismatch. However, the power consumption is very high hence, unsuitable for low power applications. Since, σ (sd) value for CMOS Thyristor and CMOS Thyristor with Footer is independent for voltage, hence it doesn't depent on the operating voltage for process mismatch. However, the value of σ (sd) needs to be improved using circuit techniques for them.

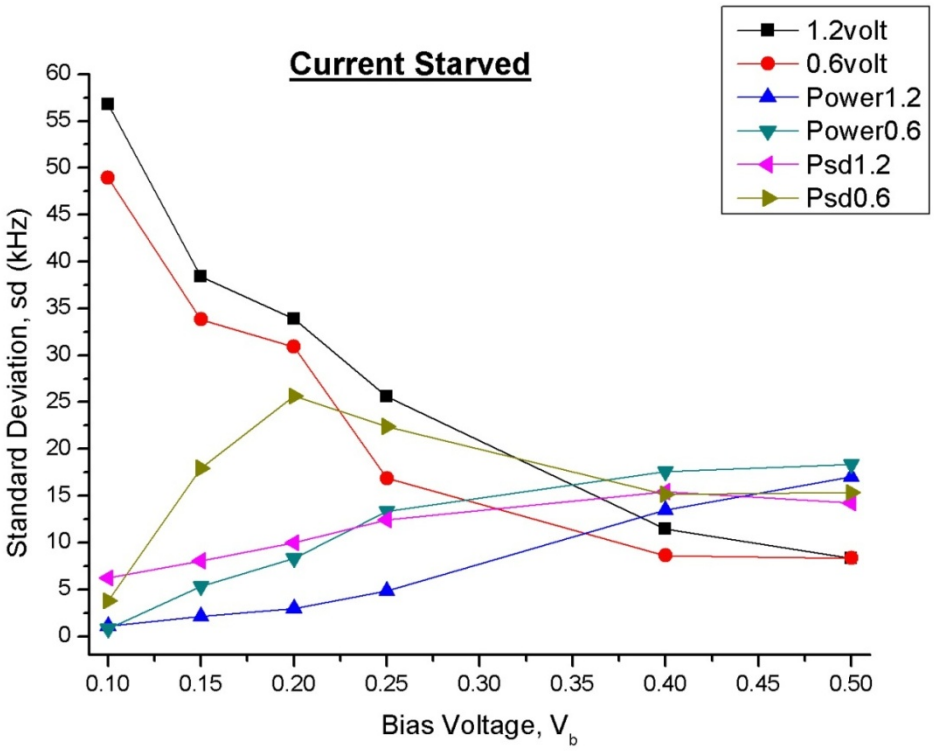
### 2.2.2 Monte Carlo Simulations at different Bias Voltages for Current Starved

| Biasing voltage, $V_b$ (volts) | Voltage, V=1.2 volts | | Voltage, V=0.6 volts | |
|---|---|---|---|---|
| | Mean, mu (kHz) | Standard Deviation (kHz) | Mean, mu (kHz) | Standard Deviation, sd (kHz) |
| 0.1 | 121.555 | 56.7641 | 107.81 | 48.9161 |
| 0.15 | 100.248 | 38.3956 | 81.0032 | 33.8097 |
| 0.2 | 103.384 | 33.9073 | 102.81 | 30.8957 |
| 0.25 | 102.27 | 25.5958 | 100.216 | 16.8544 |
| 0.4 | 98.9643 | 11.4477 | 99.0905 | 8.62507 |
| 0.5 | 98.9867 | 8.35467 | 99.1785 | 8.3428 |

**Table 2.6 Table for Monte Carlo Analysis for Current starved for diff. Biasing voltages at 100 kHz.**

### 2.2.3 σ (Standard Deviation) vs. Biasing Voltage

The curve for standard deviation vs. Biasing voltage has been plotted to get an idea of how power used can be compensated by reduced value of σ, as power increases with increase in biasing voltage whereas σ decreases and system's performance for process mismatch improves.



Here, Psd stands for the product of Power and standard deviation (σ).

1.2volt shows the value of σ for different biasing voltage for Vdd = 1.2 volts.
0.6volt shows the value of σ for different biasing voltage for Vdd = 0.6 volts.
Power1.2 shows the power consumption at Vdd = 1.2v at diff. biasing voltages.
Power0.6 shows the power consumption at Vdd = 0.6v at diff. biasing voltages.

Psd parameter was choosen to determine an optimum point for product of power and σ. However, psd curve turned out to be inconclusive.

## 2.3 Supply Sensitivity for the various configurations at different Vdd

Supply sensitivity for various configurations at different Vdd (0.3 volts/ 0.6 volts/ 1.2 volts) have been determined to study the effect of voltage variations over the oscillator. It clearly shows that CMOS Thyristor & Thyristor with Footer are least sensitive to the variations in the voltage.

### 2.3.1 Supply Voltage, Vdd = 1.2 volts

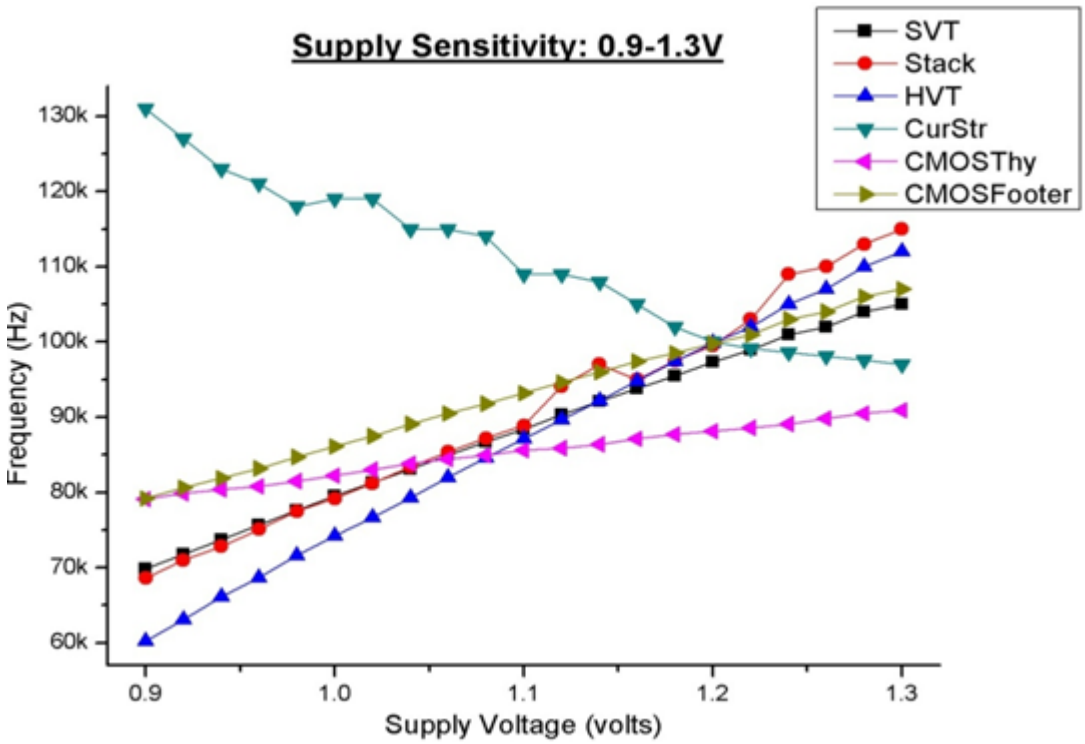



**Fig.** Supply Sensitivity around Vdd = 1.2 volts

### 2.3.2 Supply voltage, Vdd = 0.6 volts

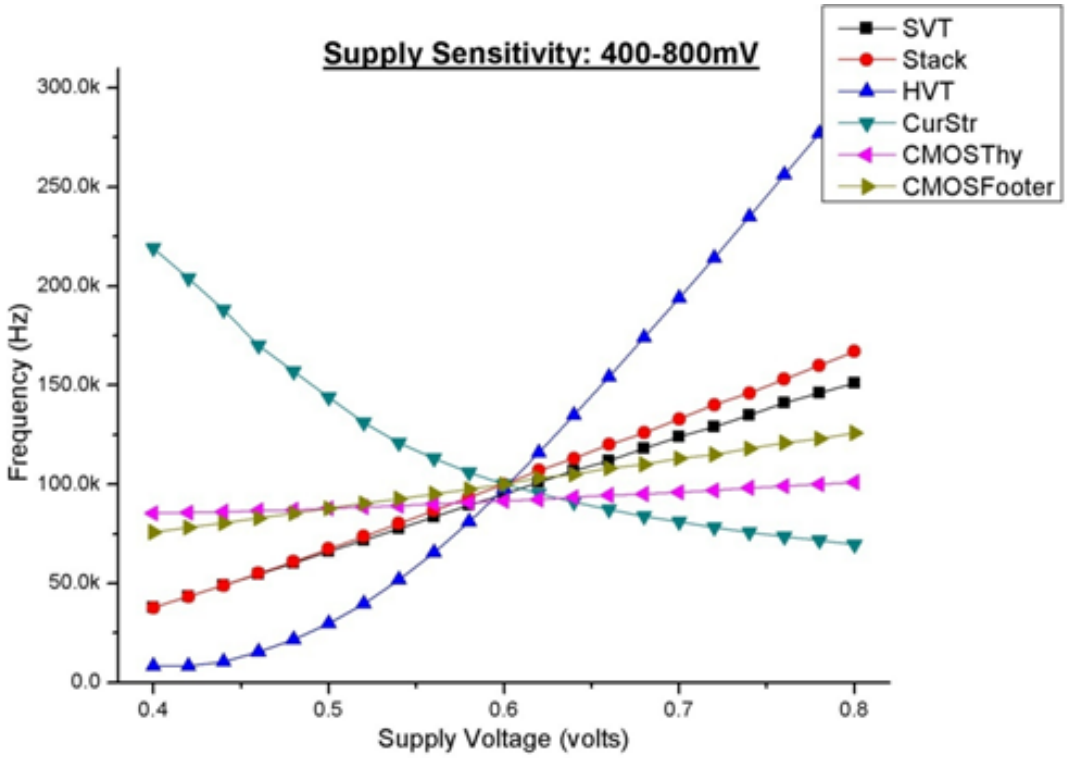



**Fig.** Supply Sensitivity around Vdd = 0.6 volts

### 2.3.3 Supply voltage, Vdd = 0.3 volts

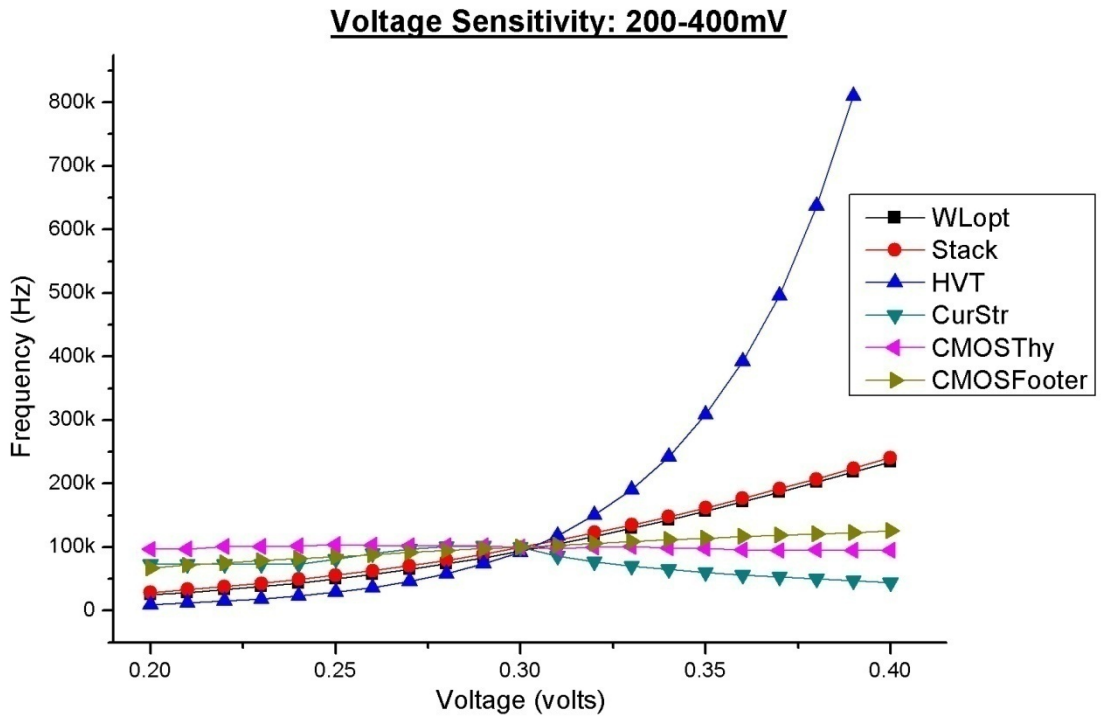



**Fig.** Supply Sensitivity around Vdd = 0.3 volts

These curves of voltage sensitivity of different configurations clearly shows that CMOS thyristor and Thyristor with Footer can be used over applications where battery life decays like DC-DC converter as they are stable over a large supply voltage range.

## 2.4 Biasing Voltage Sensitivity for Current Starved Configuration for various Vdd

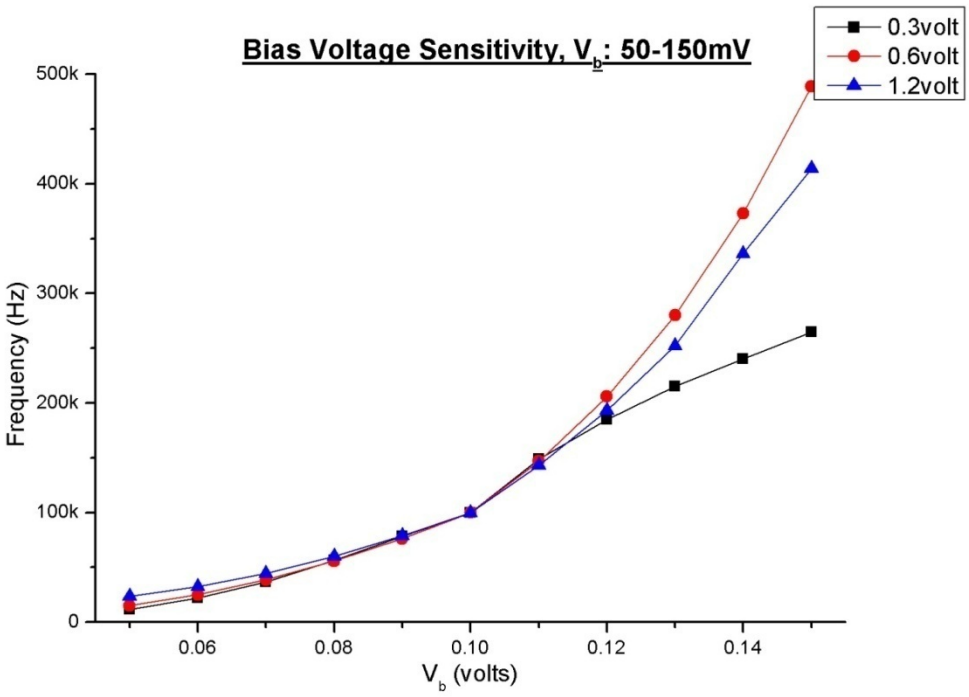



**Fig.** Biasing Voltage Sensitivity for Current starved

## 2.5 Temperature Sensitivity

Temperature sensitivity has been determined to know the effect of variations of temperature over the frequency of oscillator. It can be derived from the graphs that the Thyristor and thyristor with footer are highly sensitive to the temperature and comparable to current starved in terms of sensitivity.

Temperature sensitivity of HVt and SVt inver chains is good as compared to thyristor configurations and hence, is highly stable over large temperature range.

Temperature variations have been taken over the range of $0^{o}$C - $100^{o}$C for the analysis in the whole project.

### 2.5.1 Voltage, Vdd = 1.2 volts

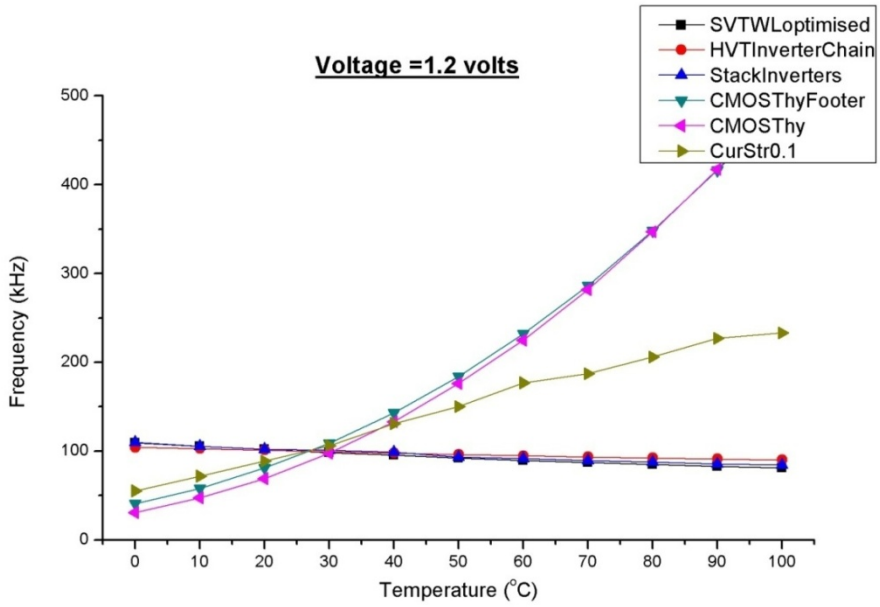



**Fig.** Temperature Sensitivity for various configs. At Vdd = 1.2 volts

### 2.5.2 Voltage, Vdd = 0.6 volts

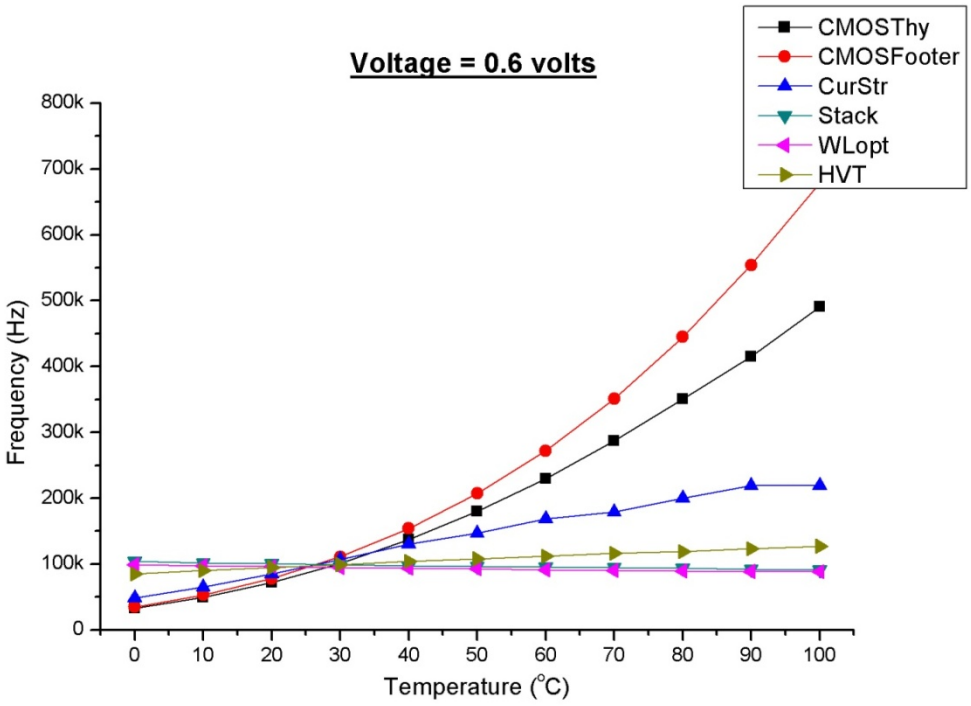



**Fig.** Temperature Sensitivity for various configs. At Vdd = 0.6 volts

### 2.5.3 Voltage, Vdd = 0.3 volts

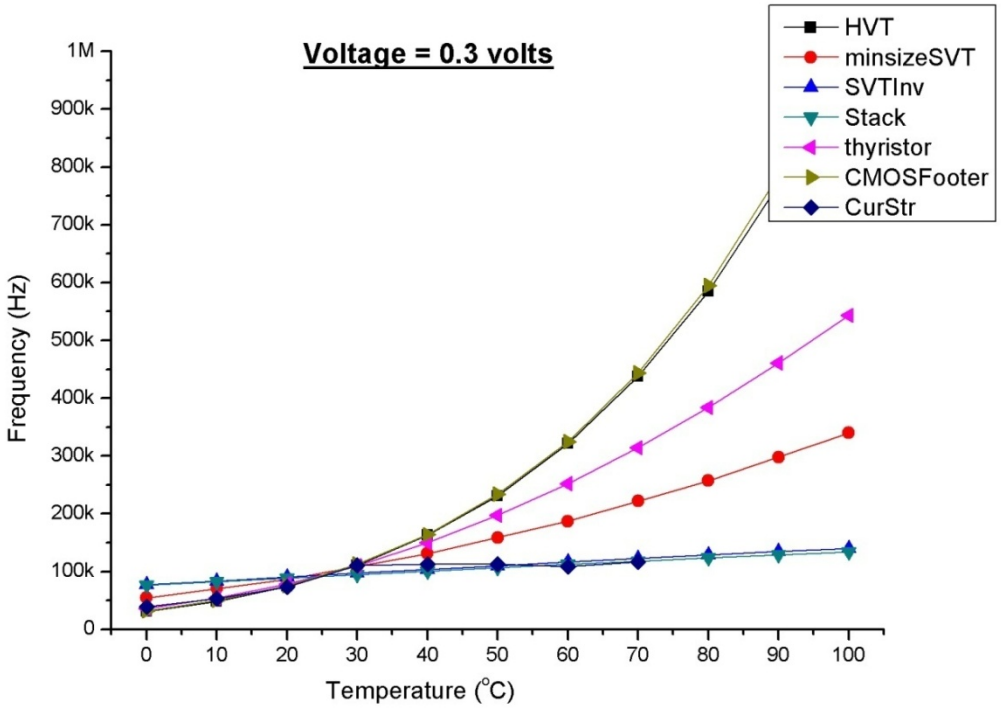



**Fig.** Temperature Sensitivity for various configs. At Vdd = 0.6 volts.

# Chapter 3 Power Consumption and Analysis of variations at frequency = 10 kHz in IBM 130nm technology

## 3.1 Power Consumption for frequency of 10 kHz for various configurations

### 3.1.1 Voltage, Vdd=1.2Volts

| Type | No. Of Inverters | W | L | Power (in nW) | Frequency (kHz) |
|---|---|---|---|---|---|
| SVT Inverter Chain | 63 | Wmin | 48.75u | 178.1 | 10 |
| HVT Inverter Chain | 37 | Wmin | 48.5u | 71.77 | 10 |
| Stack Inverter Chain | 17 | Wmin | 47.6u | 90.04 | 10 |
| Current Starved $V_b$=0.1v | 3 | 230n Wmin | 2.31u 48u | 2.851 | $\mathbf{V_{pp}}$ (0.42-1.123V) |
| CMOS Thyristor | 3 | 160n 190n | 14.9u 13.88u | 7.867 | 10 |
| CMOS Thyristor Footer | 3 | 200n 220n | 31.75u 120n | 4.933 | 10 |

**Table 3.1 Optimum Table for Minimum Power Consumption for diff. Topologies at 10 kHz at Vdd=1.2volts.**

### 3.1.2 Voltage, Vdd = 0.6 volts

| Type | No. Of Inverters | W | L | Power ( nW) | Frequency |
|---|---|---|---|---|---|
| SVT Inverter Chain | 25 | Wmin | 48.25u | 14.054 | 10 |
| HVT Inverter Chain | 7 | Wmin | 48.89u | 2.088 | 10 |
| Stack Inverter Chain | 7 | Wmin | 45.12u | 7.327 | 10 |
| Current Starved $V_b$=0.1v | 3 | 200n Wmin | 5.7u 47.1u | 1.036 | $\mathbf{V_{pp}}$ (0.17-0.49V) |
| CMOS Thyristor | 3 | Wmin | 13.32u 13.32u | 1.597 | 10 |
| CMOS Thyristor Footer | 3 | 230n 200n | 18.45u 120n | 0.936 | 10 |

**Table 3.2 Optimum Table for Minimum Power Consumption for diff. Topologies at 10 kHz at Vdd=0.6volts.**

## 3.2 Monte Carlo Analysis for various configurations

| Type | | Voltage, V=1.2 volts | | Voltage, V=0.6 volts | |
|---|---|---|---|---|---|
| | | Mean, mu | Standard Deviation, sd (in kHz) | Mean, mu (in kHz) | Standard Deviation, sd (in kHz) |
| SVT W-L Optimised | | 9.93164k | 0.479221k | 9.97186k | **0.699939k** |
| HVT Inverter | | 9.94542k | 1.43k | 10.045k | 2.27168k |
| Stacked Inverter | | 9.90516k | **0.488524k** | 9.935k | 0.705135k |
| Current Starved | $V_b$=0.1v | 10.9907k | 4.82361k | 10.3761k | 5.00513k |
| CMOS Thyristor | | 107364k | 3.5312k | 10.7015k | 3.73415k |
| CMOS Thyristor Footer | | 10.9253k | 4.64089k | 10.8267k | 4.94253k |

**Table 3.1 Table for Monte Carlo Analysis for diff. Topologies at 10 kHz.**

## 3.3 Sensitivity to the supply variations

### 3.3.1 Voltage sensitivity at 1.2 volts

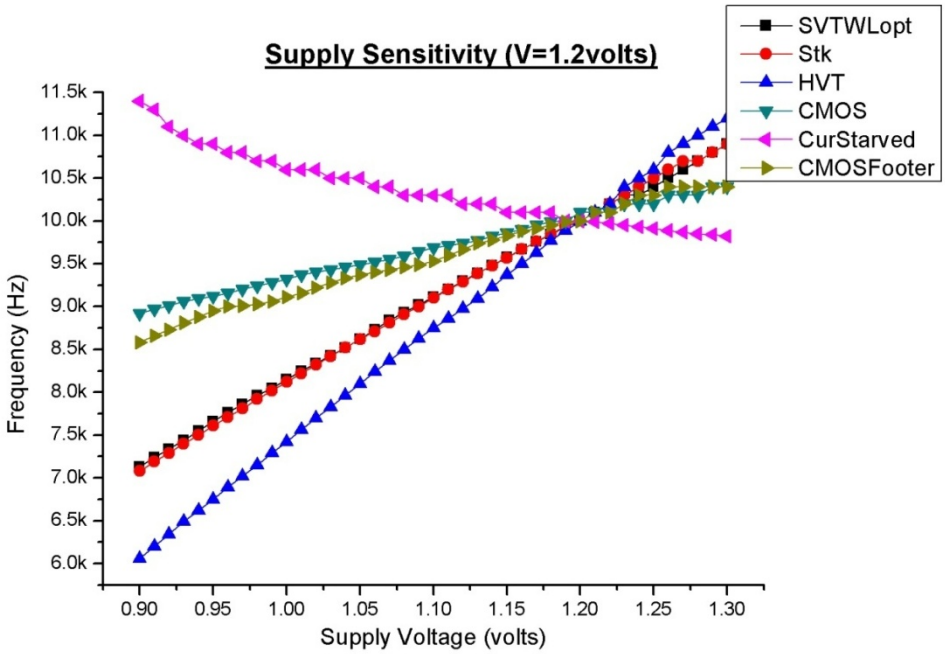



**Fig.** Supply sensitivity at 1.2 volts

### 3.3.2 Voltage sensitivity at 0.6 volts

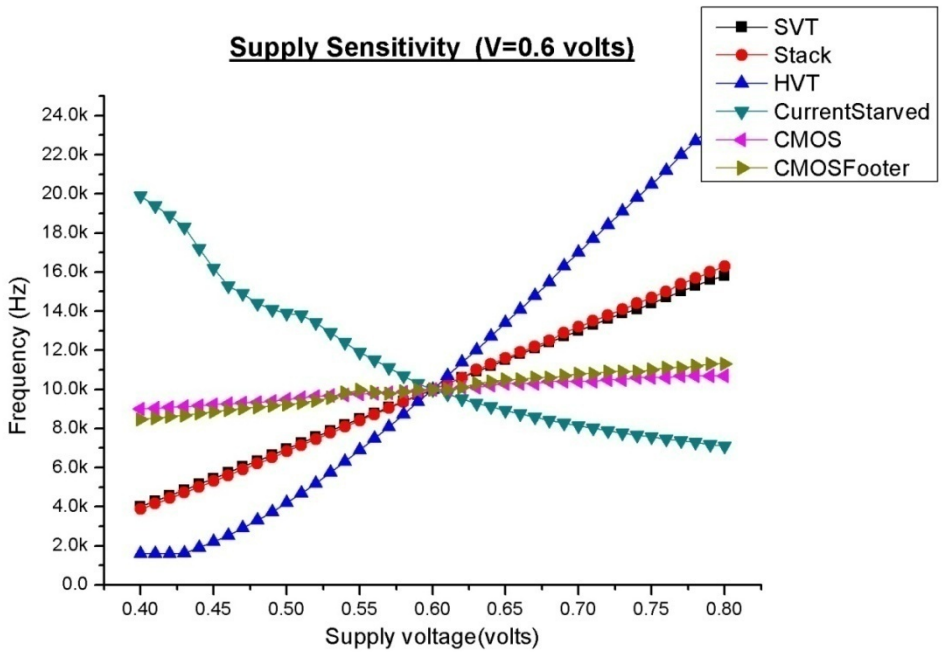



**Fig.** Supply sensitivity at 0.6 volts

## 3.4 Temperature sensitivity for variations in temperature

### 3.4.1 Temperature sensitivity at Vdd = 1.2 volts

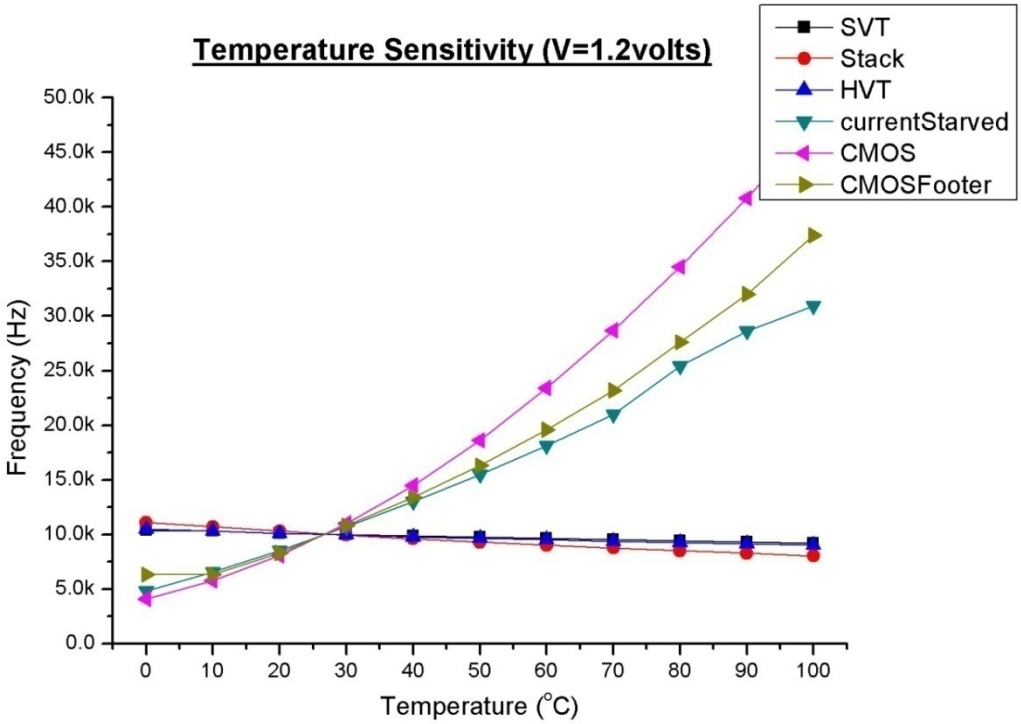



**Fig.** Temperature Sensitivity at 1.2 volts

### 3.4.2 Temperature Sensitivity at Vdd = 0.6 volts

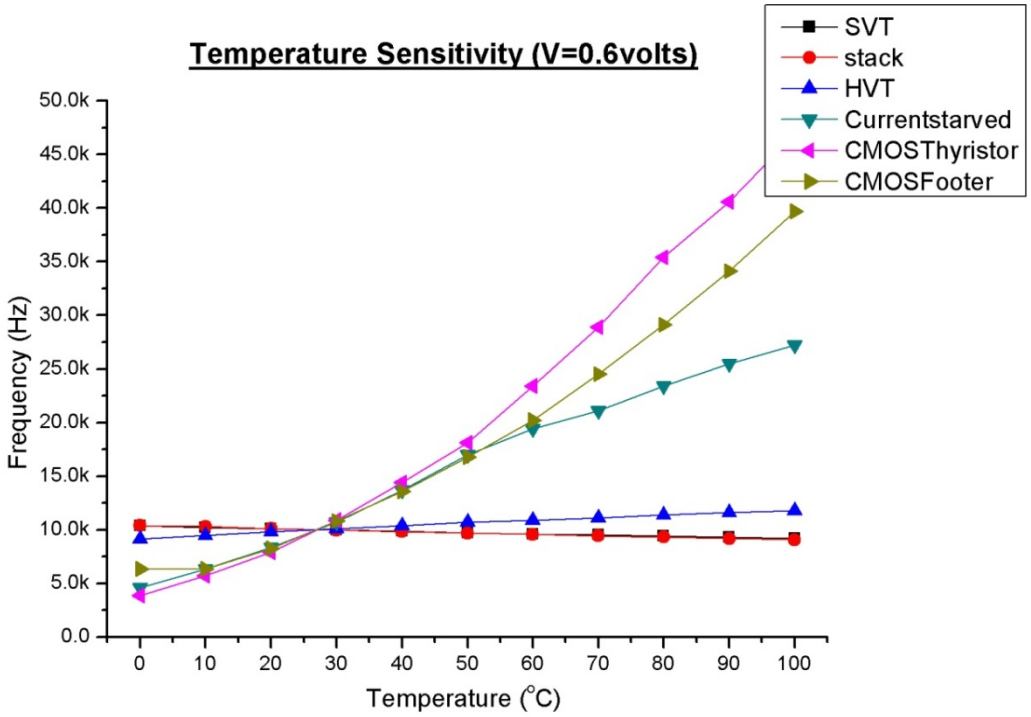



**Fig.** Temperature Sensitivity at 0.6 volts

# Chapter 4 Analysis of various Topologies in ST-65nm Technology

Since, the SVt and Stacked ring oscillator s have very high power consumption and hence, cannot be used for low power applications. In ST 65nm technology these topologies have not been explored rather, the discussion has been continued over HVt, Current Starved, CMOS Thyristor and CMOS Thyristor with Footer.

In ST 65nm Technology the **Vdd = 0.6 volts** and the whole project in ST 65nm is based on this Vdd.

## 4.1 Power Consumption for frequency of 100 kHz for various configurations

| Type | No. Of Inverter | W | | L | | | Power (nW) | Power(nW) (IBM130) |
|---|---|---|---|---|---|---|---|---|
| HVt (gp) | 3 | 120 nm | | 25.71 um | | | 12.2 | 4.738 |
| HVt (lp) | 3 | 120 nm | | 14.69 um | | | 3.159 | |
| Current Starved | 3 | 120nm | 280nm | 4.05um | 130nm | | 3.373 | 3.957 |
| CMOS Thyristor | 3 | 120nm | 120nm | 60nm | 60nm | | $382.2 \times 10^{-3}$ | 4.364 |
| CMOS Thyristor Footer | 3 | 120nm | 120nm | 60nm | 60nm | 60nm | $347.8 \times 10^{-3}$ | 1.765 |

**Table 4.1 Optimum Table for Minimum Power Consumption for diff. Topologies at 100 kHz.**

## 4.2 Power Consumption for frequency of 10 kHz for various configurations

| Type | No. Of Inverter | W | | L | | | Power (nW) | Power(nW) (IBM130) |
|---|---|---|---|---|---|---|---|---|
| HVt (gp) | 5 | 140nm | | 47.96um | | | 4.63 | 2.088 |
| HVt (lp) | 3 | 120nm | | 47um | | | $997.8 \times 10^{-3}$ | |
| Current Starved | 3 | 120nm | 120nm | 26um | 700nm | | 3.388 | 1.036 |
| CMOS Thyristor | 3 | 160nm | 170nm | 0.6um | 1um | | $144.6 \times 10^{-3}$ | 1.597 |
| CMOS Thyristor Footer | 3 | 155nm | 120nm | 1um | 120nm | 150nm | $93.37 \times 10^{-3}$ | $936 \times 10^{-3}$ |

**Table 4.2 Optimum Table for Minimum Power Consumption for diff. Topologies at 10 kHz.**

## 4.3 Comparison of Monte Carlo Results for various Topologies in IBM 130nm and ST 65nm Technology

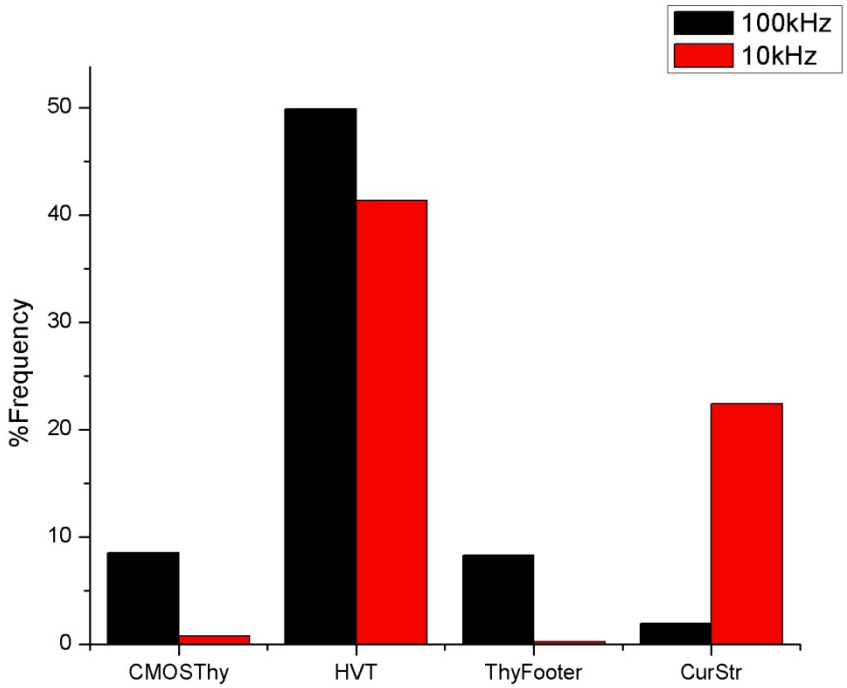
| **Type** | **Frequency = 100 kHz** | | | **Frequency = 10 kHz** | | |
|---|---|---|---|---|---|---|
| | Mean, mu | Standard Deviation, sd | Sd (IBM130) | Mean, mu | Sd | Sd (IBM130) |

| | | | | | | |
|---|---|---|---|---|---|---|
| HVt (gp) | 99.9632k | **0.39958k** | **23.8747k** | 10.0048k | **0.03660928** | **2.27168k** |
| HVt (lp) | 100.074k | 1.00861k | | 10.0633k | 56.6214 | |
| Current Starved | 96.4823k | 42.617k | 48.9161k | 20.8183k | 4.3343k | 5.00513k |
| CMOS Thyristor | 98.9233k | 42.686k | 43.1907k | 9.71423k | 1.03919k | 3.733415k |
| CMOS Thyristor Footer | 98.5847k | 42.0892k | 68.3668k | 9.7212k | 2.60528k | 4.94253k |

**Table 4.3 Optimum Table for Minimum Power Consumption for diff. Topologies at 10 kHz.**

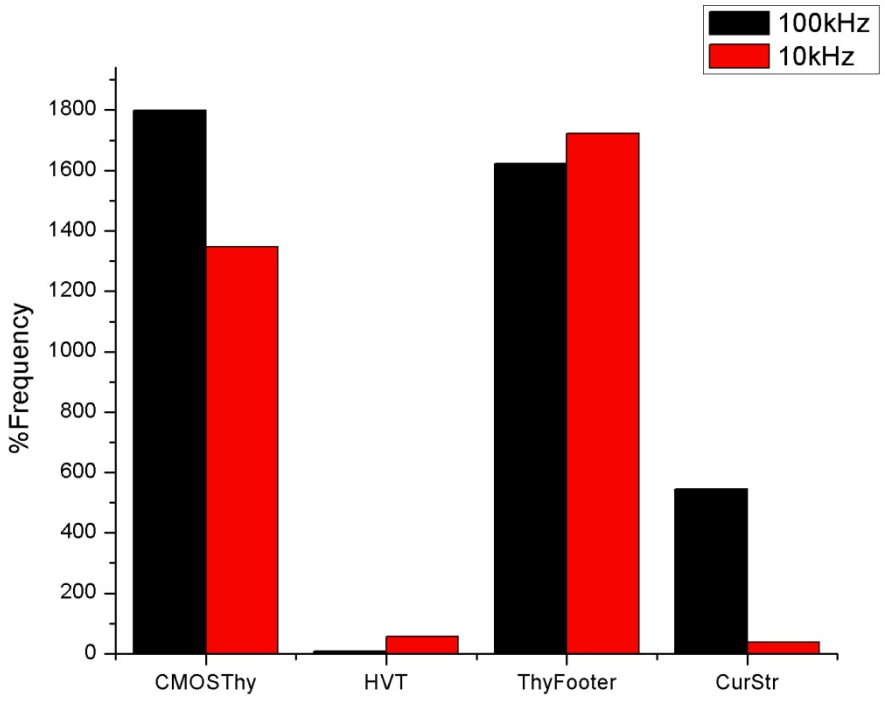
## 4.4 Comparison among the Sensitivity of various Topologies for Voltage variations

It shows the comparison between the voltage sensitivity (10% of Vdd i.e. 0.54volts-0.66 volts) of the 4 topologies at 100 kHz and 10 kHz. This indicates that the voltage sensitivity of Thyristor and Thyristor with Footer is almost nil and suit s well where, voltage variations occur.




## 4.5 Comparison among the Sensitivity of various Topologies for Temperature variations

It shows the comparison between the temperature sensitivity ($0^{o}$C-$100^{o}$C) of the 4 topologies at 100 kHz and 10 kHz. The same trend as IBM 130 follows here, as CMOS Thyristor & Thyristor with Footer are highly sensitive to the temperature, since both depend on the leakage current which is highly temperature dependent.


100kHz
10kHz
%Frequency
1800
1600
1400
1200
1000
800
600
400
200
0
CMOSThy
HVT
ThyFooter
CurStr

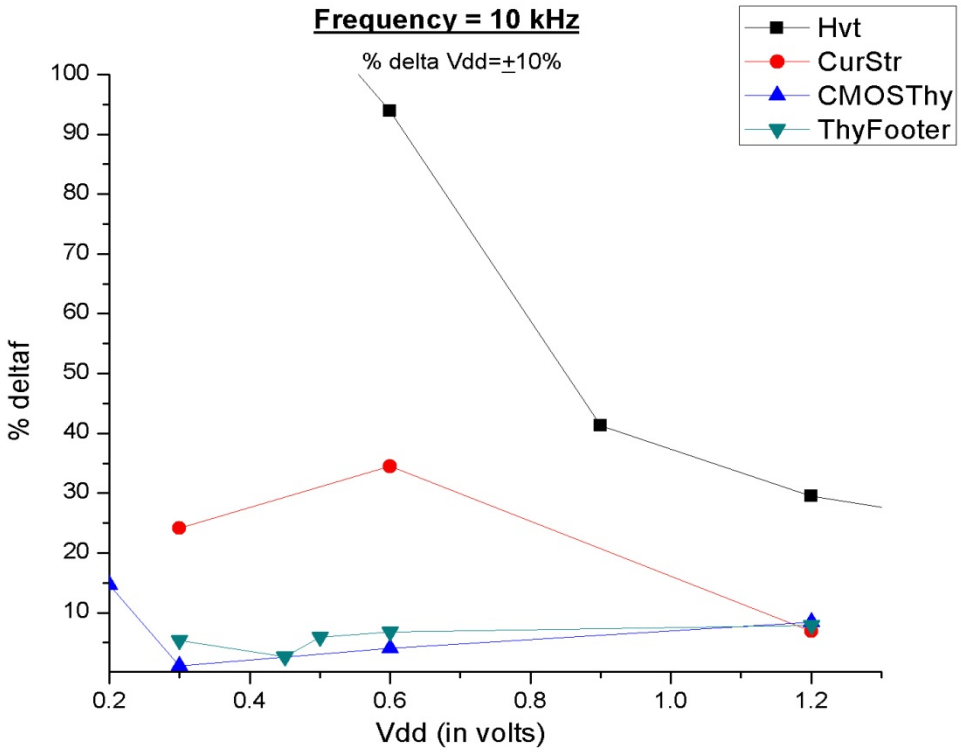
# Chapter 5 Δ f variations w.r.t ΔVdd and ΔT for 10 & 100 kHz oscillators

## 5.1 %Delta f vs. %Delta Vdd

%Δf vs. %Vdd has been obtained to determine the optimum Vdd at which frequency variation w.r.t variations in Vdd is minimum. The each coordinate in the curve represents the point corresponding to an optimum value of power consumption at particular vdd.

**%ΔVdd =** ± 10%

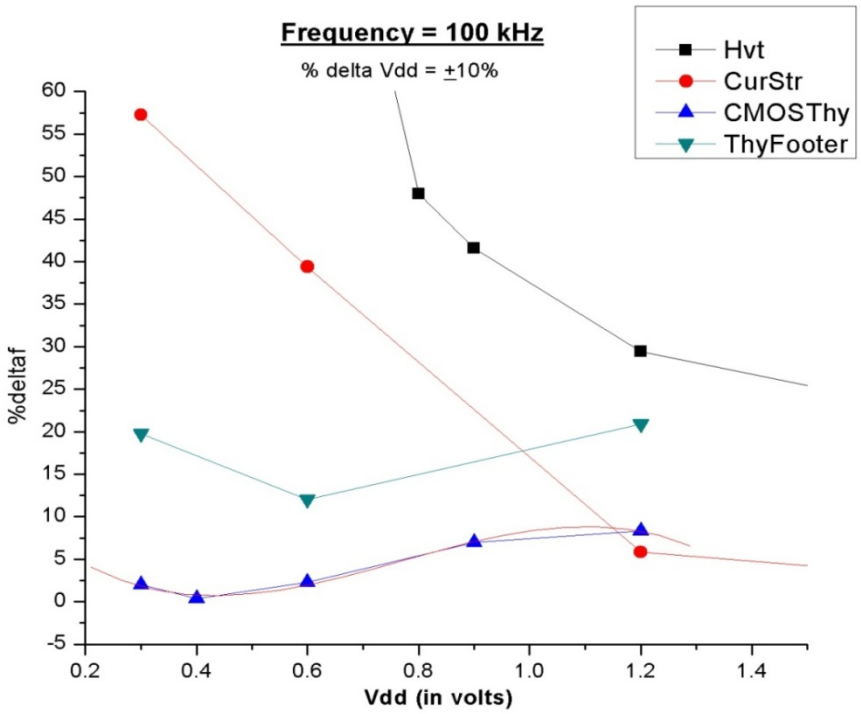
### 5.1.1 %Δf vs. %ΔVdd at frequency = 10 kHz



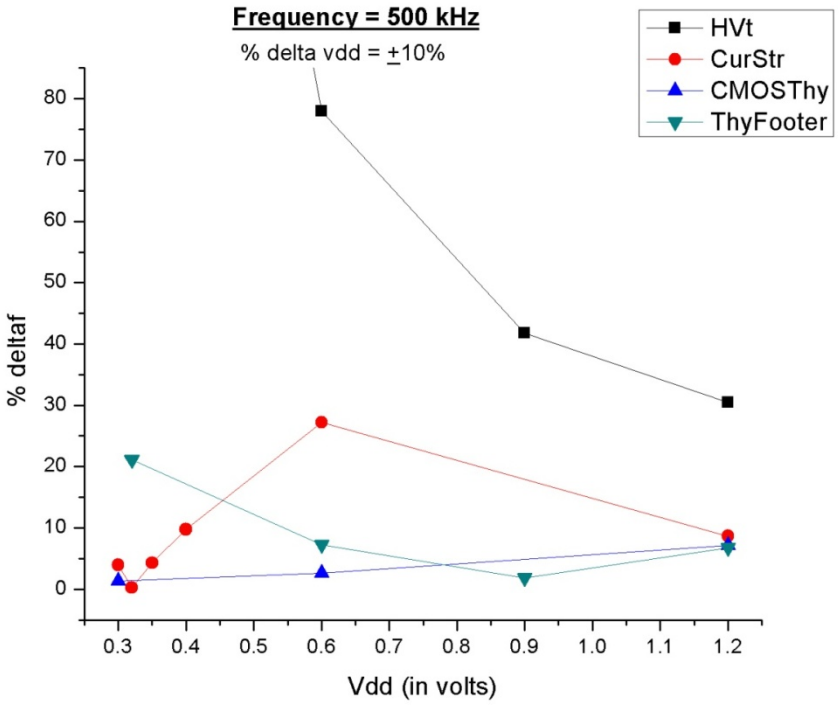

For CMOS Thyristor, Vdd ~ 0.3volts is an optimum voltage as %Δf ~ 0%.
For CMOS Thyristor with Footer, Vdd ~ 0.45 is an optimum voltage. However, optimum value for HVt & Current Starved couldn't be derived. The problem in determining the optimum point is that, since there are many parameters to be optimised to minimize the power, the points do not follow a particular trend.

### 5.1.2 %Δf vs. %ΔVdd at frequency = 100 kHz

The same trend follows for 100 kHz as well.
The optimum Vdd for CMOS Thyristor ~0.3 volts and the optimum supply voltage for CMOS Thyristor with Footer, Vdd ~ 0.5 volts.



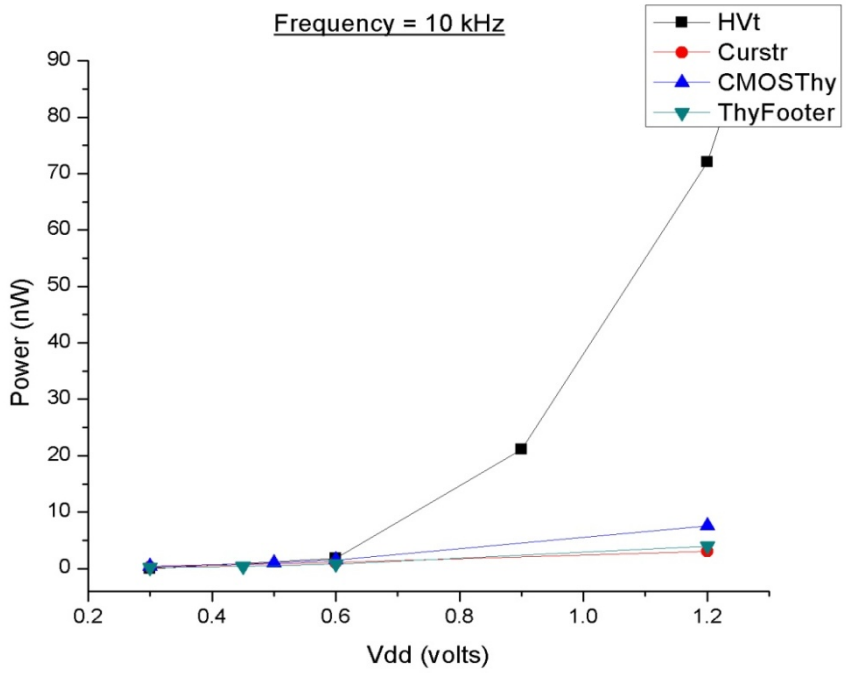

### 5.1.3 %Δf vs. %ΔVdd at frequency = 500 kHz




## 5.2 Power vs. Supply Voltage

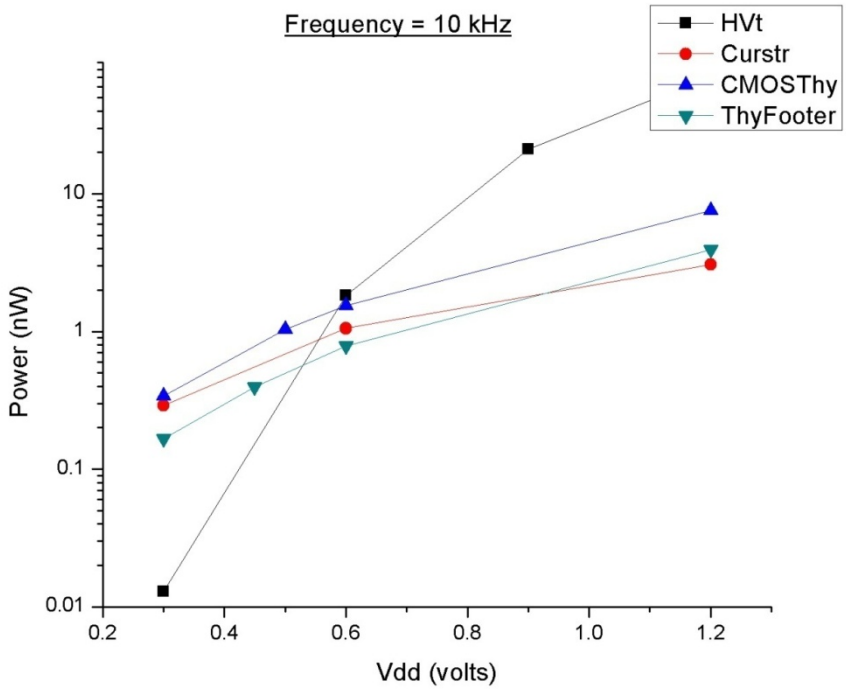
Power vs. Vdd has been determined to get an idea of how the power consumption pattern changes as the Vdd is decreased. The curve has been drawn for frequencies = 10 kHz/100 kHz/500 kHz.

### 5.2.1 Power vs. Vdd for Frequency = 10 kHz




The power decreases as Vdd reduces. However, the curve is not clear at smaller vdd ~ 0.3 volts. Hence, Curve in Log scale has been drawn .

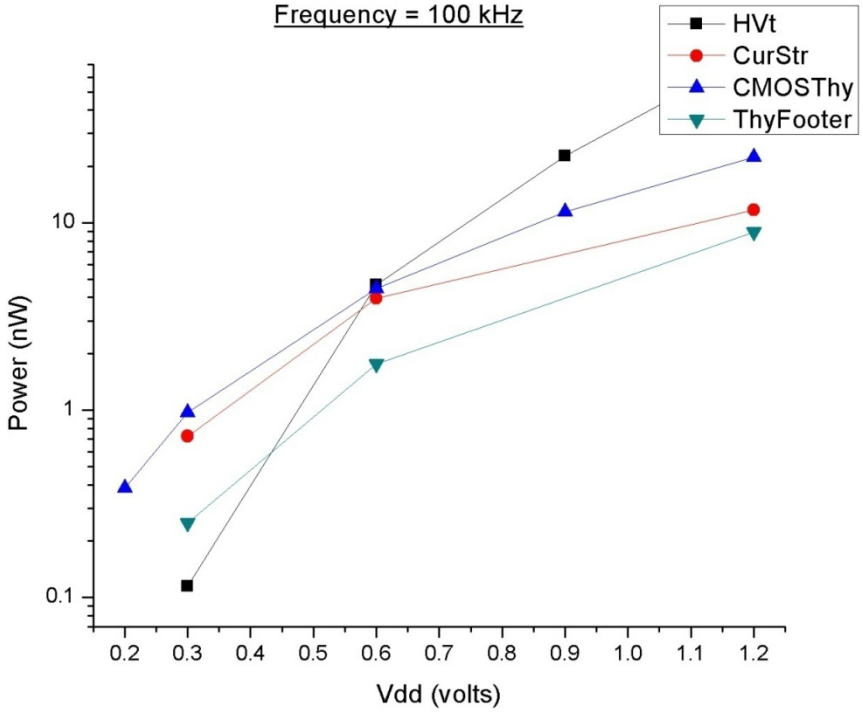
**In Log Scale**




In the graph, power consumption of HVt decreases drastically beyond 0.6 volts in comparison to the other three configurations. It gives an idea of using HVt at very low

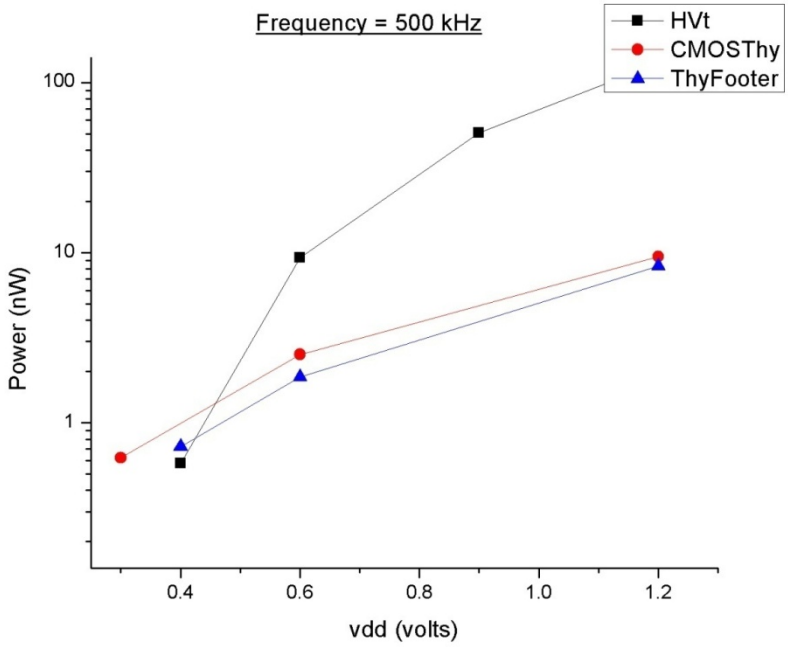
voltages ~ 0.3 volts to improve power further. This gives an idea of using High Vt transistors in the CMOS Thyristor topology to improve power further.

### 5.2.2 Power vs. Supply voltage, at Frequency = 100 kHz




The curve has been drawn in log scale to get more detailed information.
The trend for the Power vs. Vdd has been the similar for Frequency = 100 kHz as for Frequency = 10 kHz.Power used by HVt at low voltages reduces sharply.

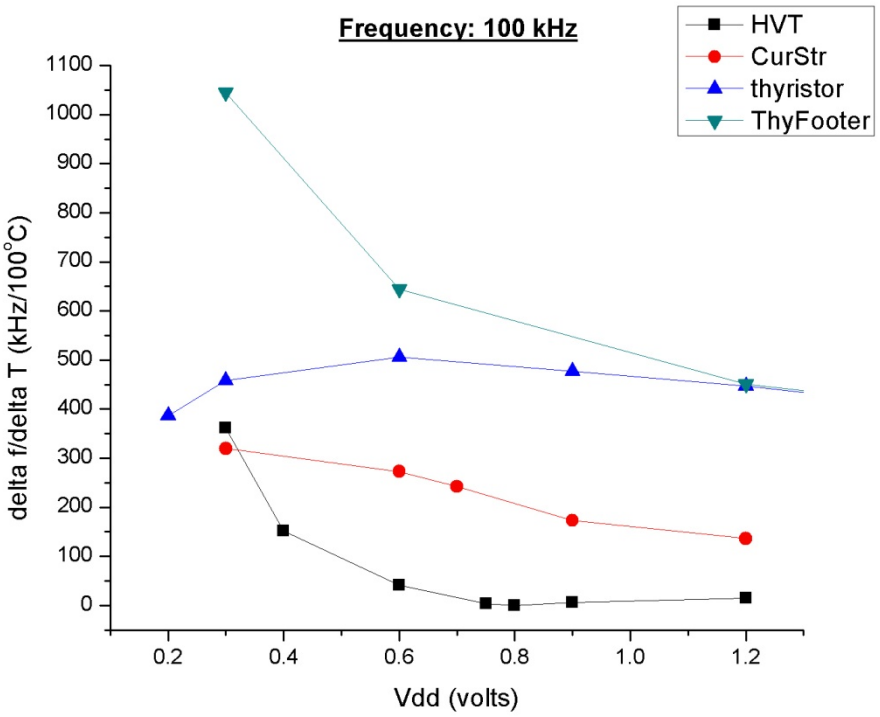
### 5.2.3 Power vs. Supply Voltage at Frequency = 500 kHz



## 5.3 Delta f vs. Delta T

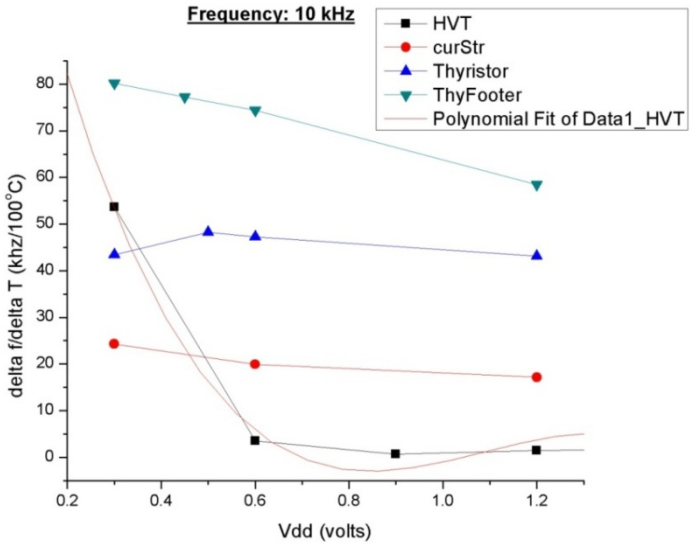
Delta f vs. Delta T curve has been determined to determine an optimum Vdd at which the change in frequency w.r.t the variations in the Temperature is minimized. The Temperature range has been taken from $0^{o}C$ – $100^{o}C$.

### 5.3.1 Delta f vs. Delta T at frequency = 100 kHz




The curve clearly indicates that the HVT has the minimum Temperature sensitivity. However, for CMOS Thyristor Temperature sensitivity is almost constant over the Vdd range (0.3v – 1.2v), which needs to be improved with better circuit design. For, current Starved the sensitivity to the variations in Temperature decreases with the increase in supply voltage.

### 5.3.2 Delta f vs. Delta T at frequency = 10 kHz




At 10 kHz, the HVt curve shows a pattern which indicates the change in frequency with the variations in Temperature would be minimum (~0 kHz/100°C) at ~ 0.75-0.8 volts. However, for the other three configurations it can not be concluded directly.

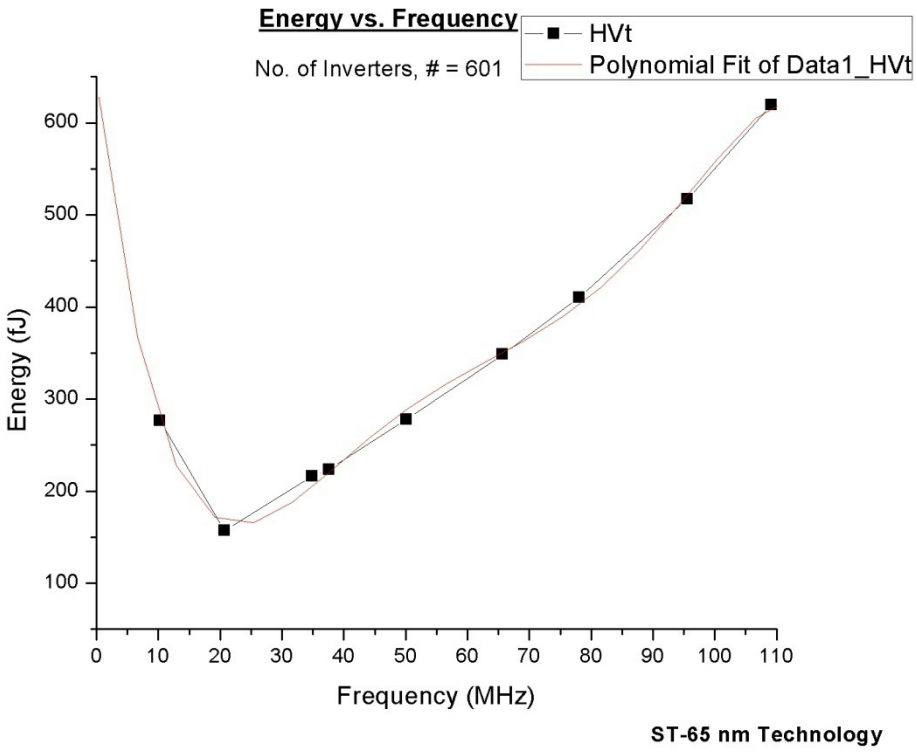
## 5.4 Energy vs. Frequency for minimum sized Topologies at ST-65nm Technology

**Motivation:** Energy vs. Frequency curve for definite number of Inverters with minimum sized is drawn to determine the frequency beyond which the power loss due to leakage becomes dominant. This helps in determining the optimum frequency of operation for a particular topology so that the energy consumed can be minimised.

The large number of inverters (e.g. # = 601) is taken with minimum sized inverters so that power consumption due to leakage becomes dominant. Otherwise, the power loss due to leakage do not becomes dominant in lesser number of inverters like 3-5.

### 5.4.1 HVt Inverter Chain

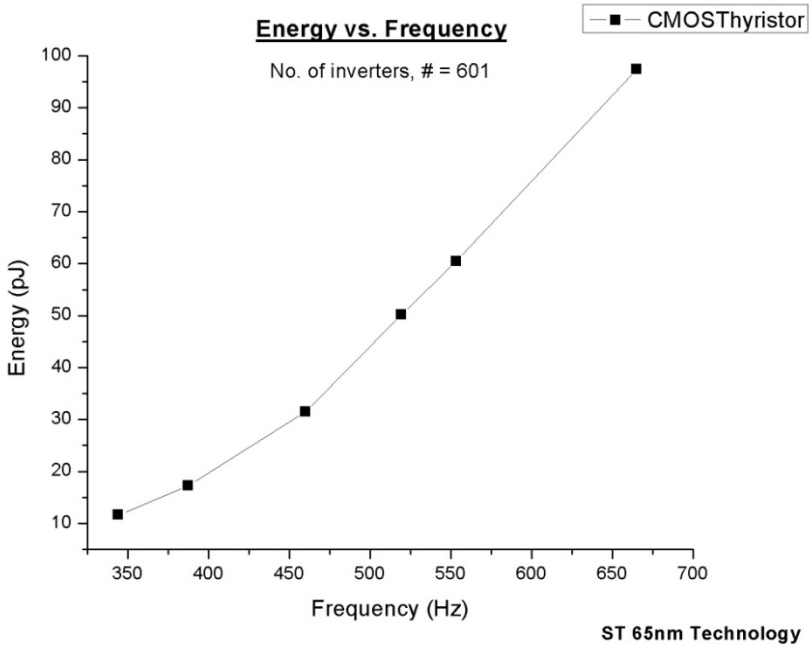
Length = Lmin = 60 nm
Width = Wmin = 120 nm




This curve clearly indicates that the optimum operating frequency for High Vt transistors (HVT) Inverter Chain is ~20 MHz as energy consumption is minimum. Beyond 20MHz leakage power becomes dominant.

### 5.4.2 CMOS Thyristor Inverter Chain

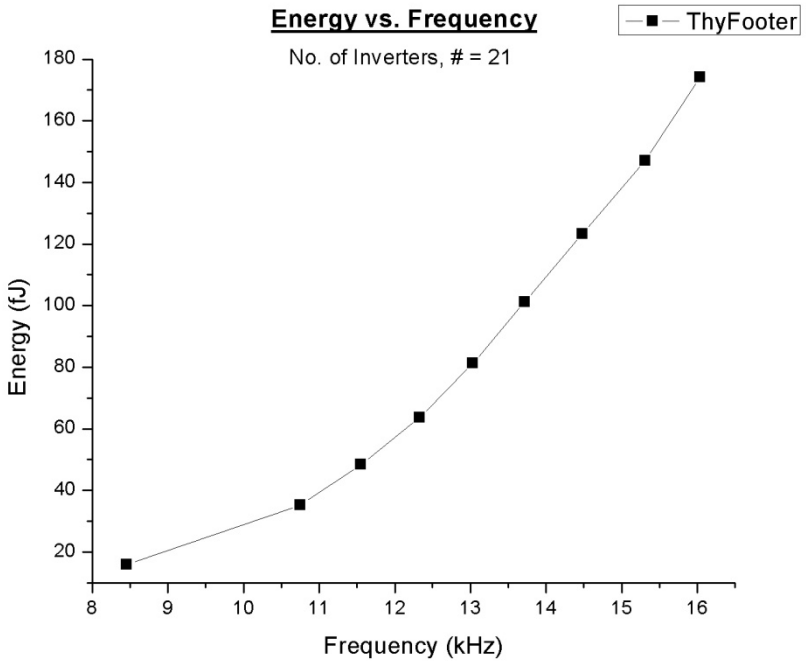
Length = Lmin = 60 nm
Width = Wmin = 120 nm



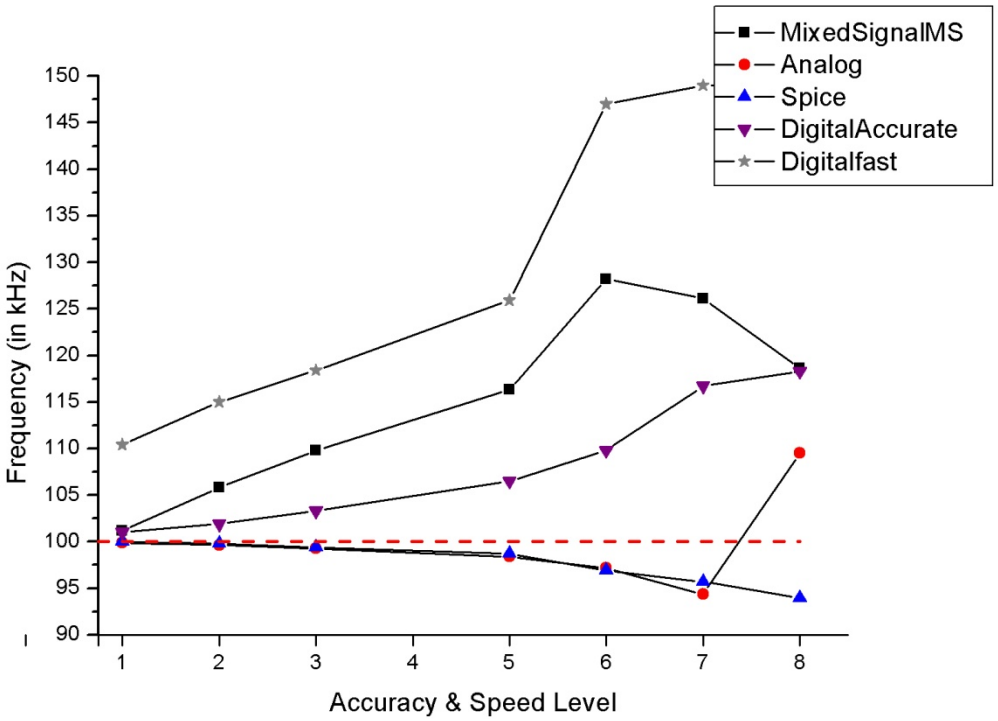
The curve shows, that either the optimum frequency of operation for the CMOS Thyristor Topology exist beyond 300Hz or it is difficult to be determined.

### 5.4.3 CMOS Thyristor with Footer

Length = Lmin = 60 nm
Width = Wmin = 120 nm



# Chapter 6 Comparison for the Different Simulation Options in UltraSim




**Motivation:** For a particular simulation using UltraSim the result I obtained was 100 kHz and when I simulated the same circuit on Spectre, the result obtained was 82 kHz. This led to the inspection of the different options available in the UltraSim and it clearly revealed that the accuracy of UltraSim depends on the options selected.

The default settings for UltaSim are: **Mixed Signal MS**
**(Speed & Accuracy Level = 5)**

In the graph, Red Doted line shows the simulation result obtained from the Spectre simulations. The accuracy & speed level for all the 5 options in UltraSim has been varied. The graph clearly shows that:

- Digital Accurate shows better results than the default settings (Mixed Signal).
- Ana log option shows the best results with least error from the Spectre simulations.
- Aggressive (speed & accuracy level = 8) shows better results than Aggressive (speed & accuracy level = 6 and 7) for Mixed Signal.

# Chapter 7 Conclusion

- The Power consumption in the CMOS Thyristor with Footer topology is the least.
- CMOS Thyristor and CMOS Thyristor with Footer are insensitive to the variations in the supply and can be used as an ideal configuration for DC-DC converters etc., where voltage supply from battery reduces with the time.
- However, both the configurations have a very poor Temperature sensitivity and are highly vulnerable to the variations in the temperature and hence, cannot be used temperature specific applications.
- As the Technology scales down from IBM 130nm to ST 65 nm Technology the power consumption for CMOS Thyristor & CMOS Thyristor with Footer reduces by ~ 90 %.
- While scaling down the technology from IBM130nm to ST 65mn the power consumption for HVt inverter chain topology has reduced by ~50% - 60%. Moreover, the value of sigma (standard Deviation) has decreased by ~ 25x – 40X .

## 7.1 Possible Solutions for Current Problems

### 7.1.1 To Reduce Power Further

To reduce power high vt transistors can be used with CMOS Thyristor and CMOS thyristor with Footer topology to reduce power further.

### 7.1.2 To Reduce Sensitivity to the variations in Temperature & Voltage

CMOS thyristor and CMOS Thyristor with Footer configurations are leakage dependent and hence, do not depend on the operating voltage. As a result, their voltage sensitivity is too good. However, their temperature sensitivity is highly temperature dependent, since leakage current in the MOSFETs exponentially depend on the Temperature.

HVT MOSFETs are lesser temperature sensitive as compared to simple Vt (low Vt) MOSFETs.

- High Vt MOSFETs can be used in the design of CMOS Thyristor and Thyristor with Footer to make them lesser temperature sensitive. However, it reduces the performance of the system (speed), hence, HVt can be used at leakage dependent MOSFETs and Simple Vt can be used at other locations of the design to improve the performance of the system.
- Newer biasing design has to be developed for the CMOS Thyristor so that the leakage current flowing in the system is a controlled (regulated) current and as a result, the system becomes insensitive to the temperature variations.

### 7.1.3 To improve overall performance of the Topology

To improve the overall performance of the topology, the topology should be operated around its "sweet point" (its "optimum point") where the system has the best performance. This will improve the efficiency of the system.

- Since, the power consumption by HVt Inverter Chain reduces drastically when it is being operated in sub-threshold region, hence its better to operate it below 0.4 volts.

- This property can be used in even in CMOS Thyristor Design as well as CMOS Thyristor with Footer Design, by using High Vt transistors in place of Simple Vt (SVT) transistors and reduce, the power consumption further.

## 7.2 New Designs Proposed

Some of the modified designs have been proposed by the research group to improve the performance of the ring oscillator.

### 7.2.1 Using HVt transistors in CMOS Thyristor

Since, the power consumption in case of high Vt transistors at voltage below 0.5 volts (sub threshold region) is too low in comparison to the CMOS Thyristor and Thyristor with footer designs, HVt transistors can be used in place of simple Vt transistors in CMOS Thyristor design.
Hence, four cases has been explored in terms of their sensitivities and effect of Process Mismatch over their performance through Monte Carlo Analysis.
Case 1: SVT + SVT transistors in CMOS Thyristor design. (**Original Design**)
Case 2: HVT + HVT transistors in CMOS Thyristor design.
Case 3: SVT + HVT transistors in CMOS Thyristor design.
Case 4: HVT + SVT transistors in CMOS Thyristor design.

**Optimum Power consumption by 4 cases**

| Type(CMOS Thyristor) | No. Of Inverters | W | | L | | Power (W) | Frequency (kHz) |
|---|---|---|---|---|---|---|---|
| SVT + SVT (original Design) | 3 | 160nm | 170nm | 0.6um | 1um | 144.6p | 10k |
| HVT + HVT | 3 | 120nm | 120nm | 138nm | 60nm | 33.34p | 10k |
| SVT + HVT | 3 | 120nm | 560nm | 60nm | 115nm | 70.81p | 10k |
| HVT + SVT | 3 | 120nm | 120nm | 245nm | 60nm | 201.7p | 10k |

**Comparison of Monte Carlo Results and %Δf w.r.t variations in Temperature & voltage**

The whole analysis has been been done using,
Vdd = 0.6 volts and frequency = 10 kHz.
$\Delta T = 0^oC - 100^oC$
$\%\Delta Vdd = \pm 10\%$

| Type | Monte Carlo Results | | %Δf w.r.t %ΔVdd | Δf w.r.t %ΔT |
|---|---|---|---|---|
| | Mean | Standard Deviation, σ | | |
| SVT + SVT (original Design) | 9.71423k | 1.03919k | 0.78% | 134.806k |
| HVT + HVT | 10.5058k | 2.58705k | 4.15% | 183.09k |
| SVT + HVT | 10.4346k | 2.42534k | 5.41% | 222.441k |
| HVT + SVT | 9.86447k | 3.80032k | 15.37% | 180.973k |

**Inference**

The power has been reduced by ~ 80% by using HVT transistors in place of simple Vt transistors in CMOS Thyristor design at 0.6 volts. Which can be further be improved by using smaller values of Vdd. However, there has not been any improvement in terms of sensitivity for the variations in voltage and temperature. This indicates that to improve the performance of the system in terms of process and environment variations we have to look for some other better circuit design.

### 7.2.2 Adding another transistor in CMOS Thyristor Design

Adding another transistor in CMOS Thyristor design has been proposed to compensate for mismatch between the inverting transistors and hence, to improve the performance of the Oscillator.

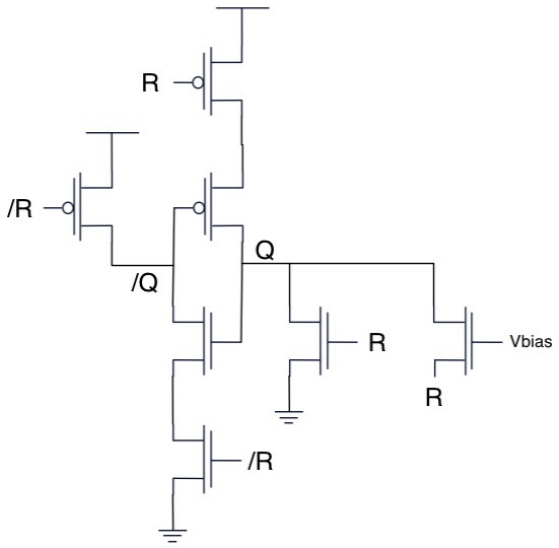



**Fig.** New Modified Design to improve the process Mismatch problem

Here, the biasing voltage can be controlled externally which controls the voltage at Q and hence, voltage level at q is not floating during the floating stage of the delay cell.

Such new designs have to be explored in future to improve the performance of the ring oscillators or clocks. Exploring such designs will form the next level to this project and will form the basis for the future research.