CMOS Thyristor Based Low Frequency Ring Oscillator

Submitted by:

PIYUSH KESHRI
4th year Undergraduate Student
Electrical Engineering Dept.
IIT Kanpur

BIPLAB DEKA
4th year Undergraduate Student
Electrical Engineering Dept.
IIT Kanpur

Abstract

In the Era of digital World, low power applications are the needs of the market to save the resources. Delay elements (e.g. digital clock) are essential parts of such digital applications. Hence, generation of such low power clocks is a major issue of research.

Precise clock generation independent of supply and temperature sensitivity has been the main objective in various applications such as DC-DC converters. Precise delay can be generated using ring oscillators by using the symmetry of the oscillator ring.

Ring oscillators have been used because of their ease of implementation, wide tuning ranges, operating at low voltages and existing possibility of complete integration in standard CMOS processes. They also occupy smaller chip area.

This project has been aimed at designing a clock with low power, low frequency, and low operating voltage using ring oscillator topology. It aims at determining the best possible configuration for the ring oscillators having the least power consumption and precise delay with lesser sensitivity to the variations in the temperature and supply voltage for frequencies of ~1 kHz. The oscillator configurations have been designed at frequency of 1 kHz for TSMC-0.18µm CMOS Technology.

The design of clock using ring oscillator of a wide range, low sensitivity to the variations of the supply, but mainly low power consumption has been detailed in this work. The various topologies of ring oscillators like simple Vt Inverter Chain, Current Starved Simple Inverter Chain, CMOS Thyristor and CMOS Thyristor with footer have been explored in this project, to determine the sensitivities of each topology w.r.t variations in the temperature and supply.

1. Introduction

The aim of this project is to develop a low power clock for low frequencies in the order of 1 kHz.

The typical design of ring oscillators consists of odd number of inverters used as delay cells connected in cascade and in a closed loop, which provide enough gain and phase shift to satisfy the Barkhausen's oscillation criteria.

In these topologies the oscillation frequency is given by:

$$f = \frac{1}{2N\tau_d}$$

Where, N is the number of delay cells in the ring and τ_d is the delay time in the cell.

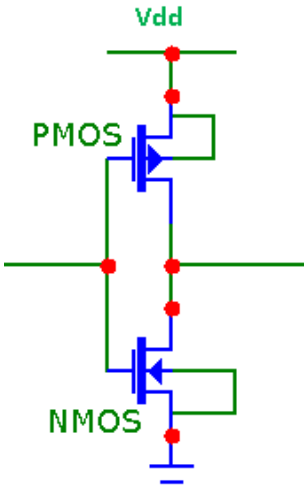


Fig. 1(a) CMOS Inverter

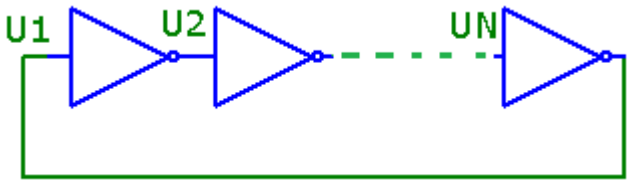
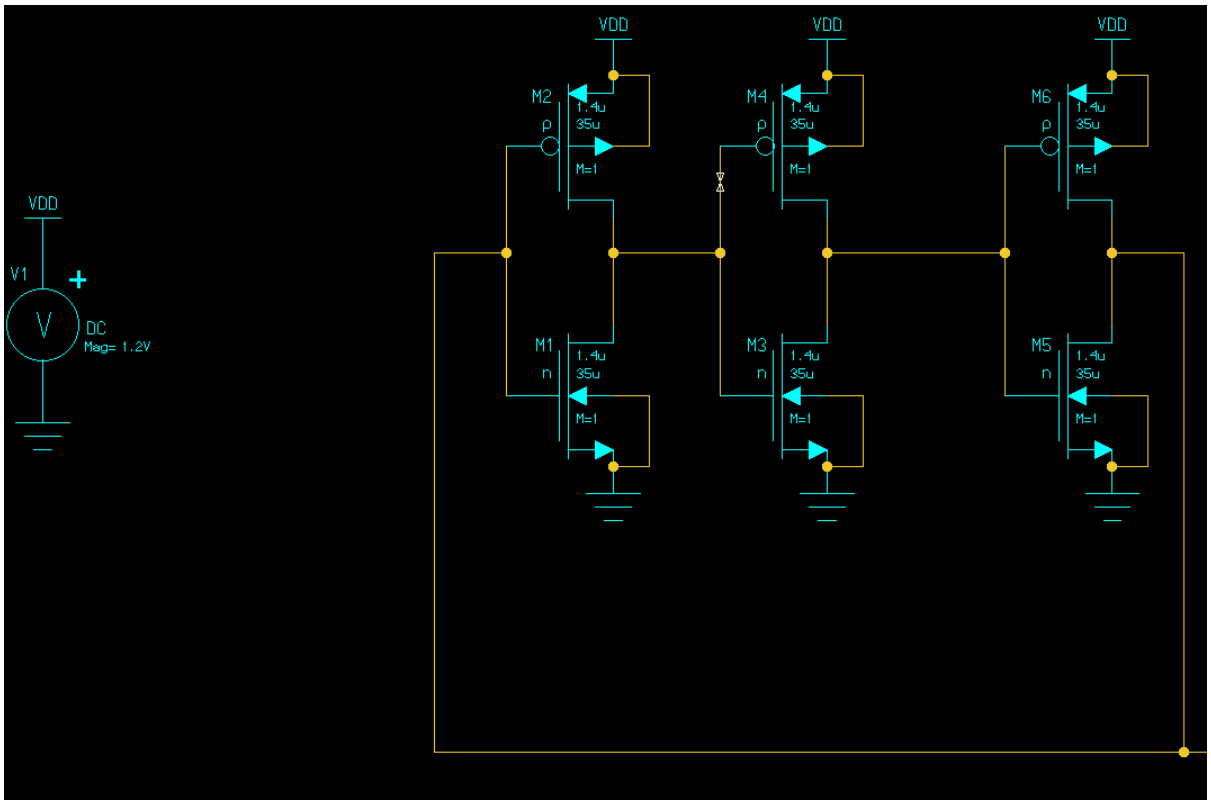


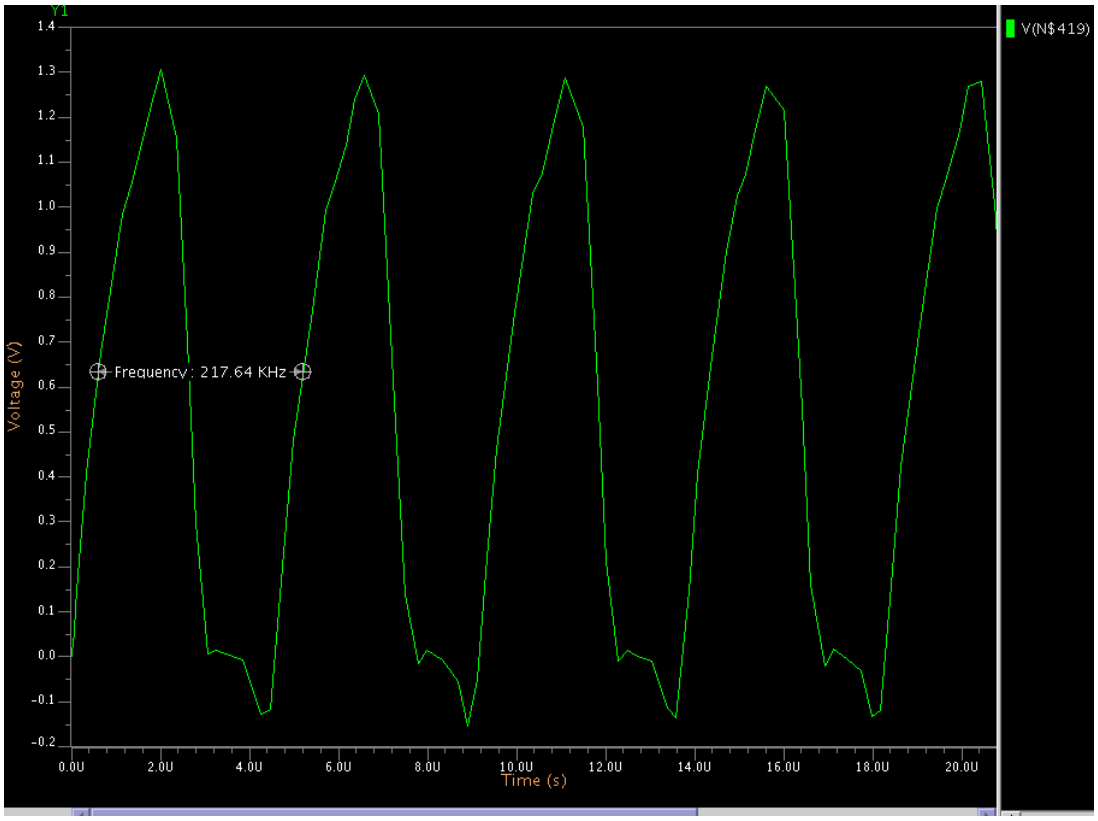
Fig. 1(b) Inverter Chain to form Ring Oscillator

In section 2 we look at the design of ring oscillators based on an inverter chain and justify why it is not possible to use such a design for designing clocks in this frequency range. In section 3 we describe a modification that can be made to the abovementioned inverter based ring oscillator. In section 4 we describe a thyristor based design.

2. SVT(Simple V_t) Transistor Inverter Chain

The simplest oscillator is based on the usage on a chain of odd number of inverters. Output of such a SVT inverter chain with three inverters is shown below.





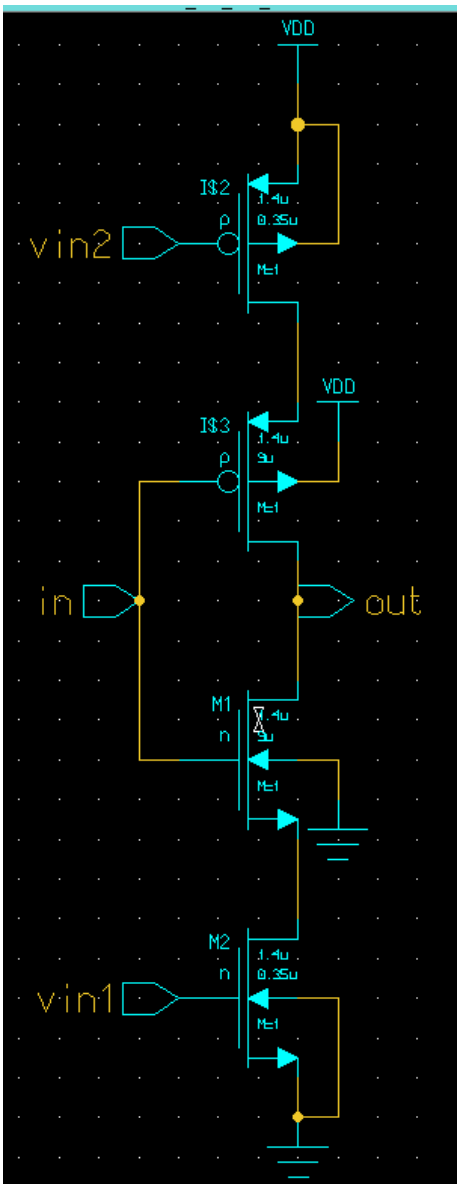
As we can see the frequency of this oscillator is 217 kHz which is much higher than our desired frequency. We conclude that the delay provided by such a small number of transistors is not adequate. The solution to this problem is to use more number of transistors or to decrease their (W/L) ratio.

Keeping (W/L) ratio constant we find that we need 601 inverters to reach a frequency of 1.057 kHz. This is not a feasible solution due to the large number of inverters used which increases the power consumption and chip area. The power consumption in this example was 716 nW.

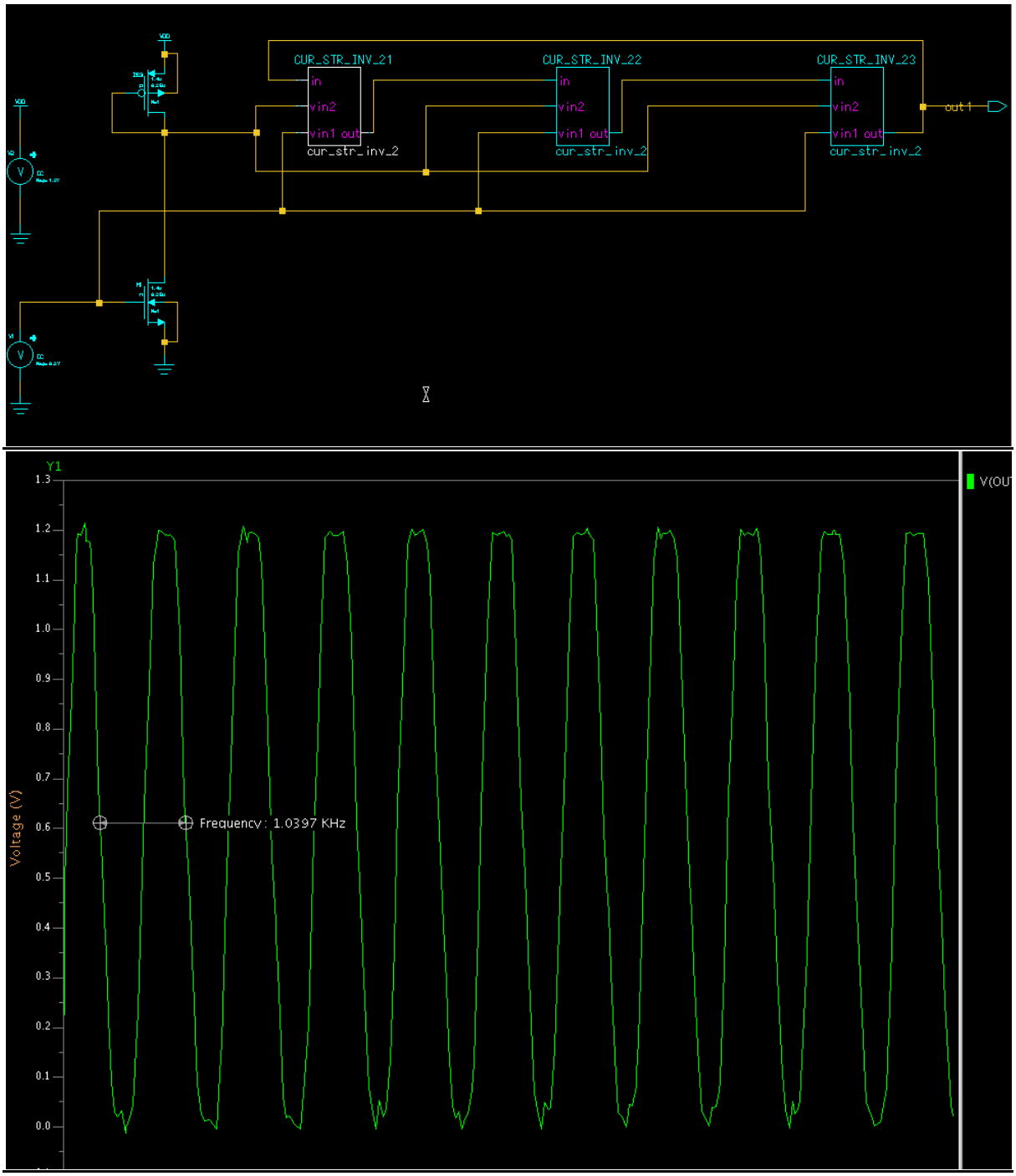
3. Current Starved Inverter Chain

In order to increase the delay provided by each inverter we use the current starved design shown below. This design limits the current available to charge/discharge the capacitances when the output of the inverter changes. By doing this we increase the delay provided by each inverter.

Starving is done using biasing circuit which the delay of each cell depending upon the extent of starving based on the biasing voltage and the scaling of the MOSFETs. It also improves the efficiency of the system by reducing the power consumption.

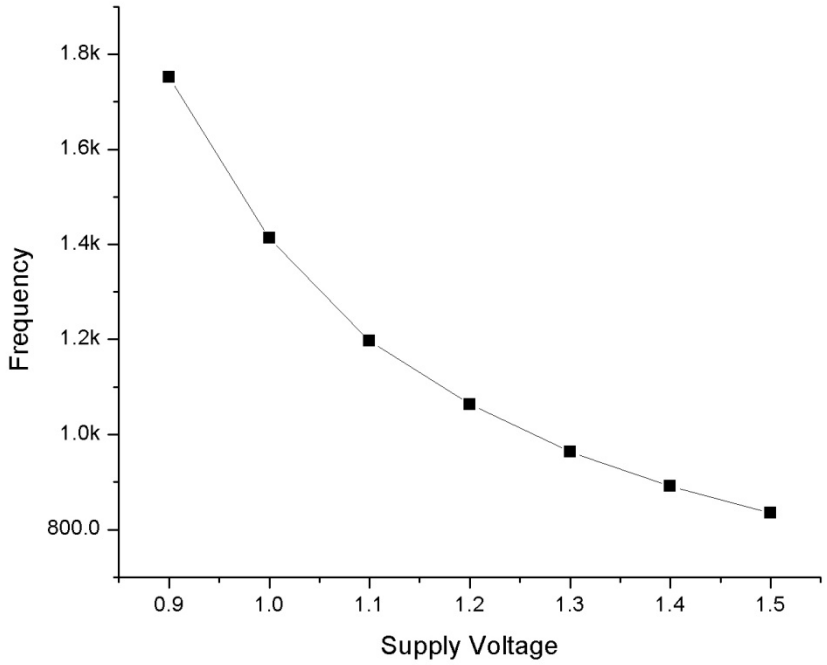


We designed a circuit using only three such current starved inverters and were able to get the desired frequency of oscillation. The biasing voltage decides the current available drain current in each inverter and hence can be used to control the frequency of operation.



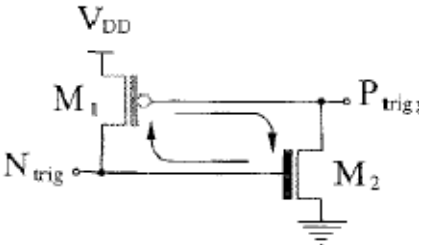
The power consumed by this circuit is 2.9 nW as compared to 716 nW of the previous design.

Although this circuit helps us achieve our desired frequency with very low power consumption, this circuit has the drawback that the output frequency is highly dependent on the supply voltage. A plot of frequency vs supply voltage is shown below.



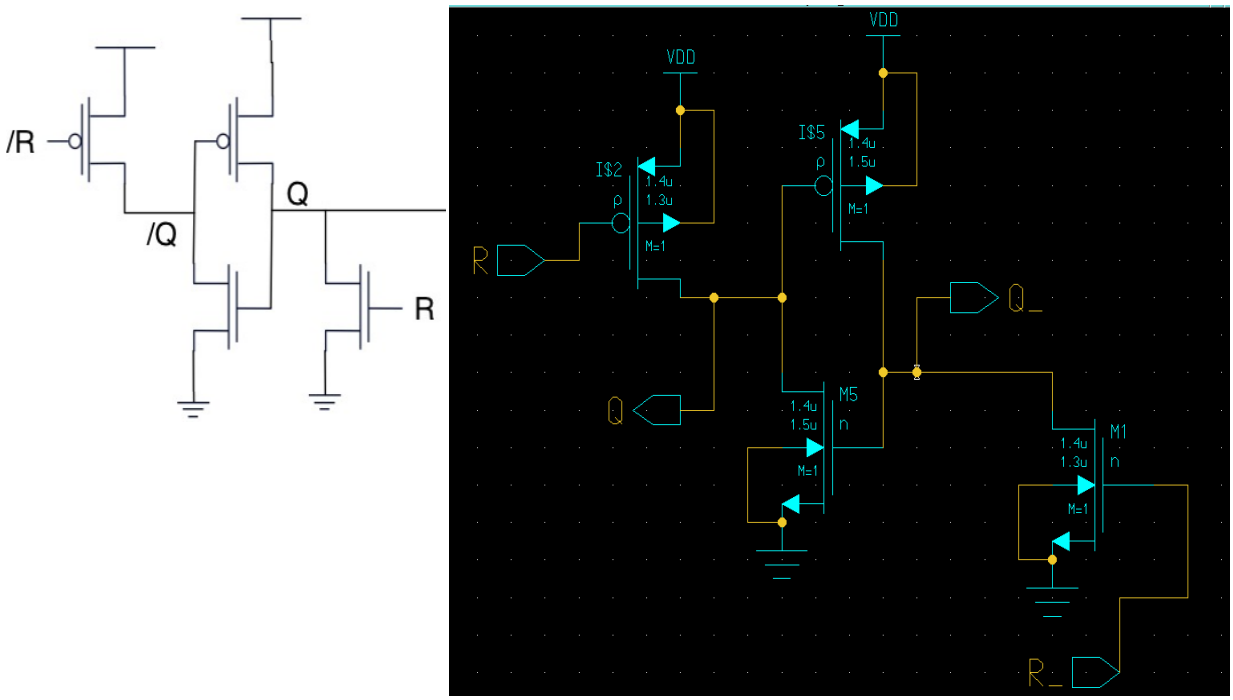
4. CMOS Thyristor Based Inverter

In order to solve the above problem we used a CMOS thyristor based inverter. It is considered to be less sensitive to conditions like voltage as it depends on leakage current and not on voltage of operation. Also this delay element doesn't consume any static power and its power consumption decreases with increasing delay value. Its operation can be explained with the help of the figure given below:

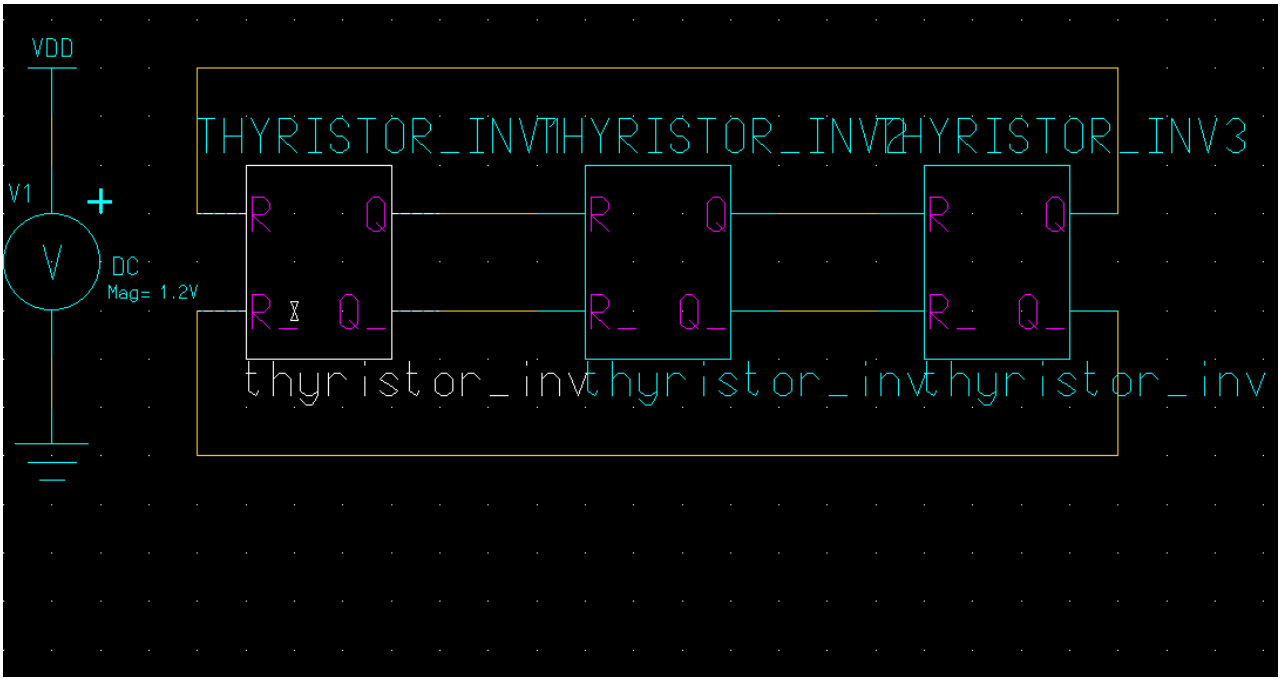


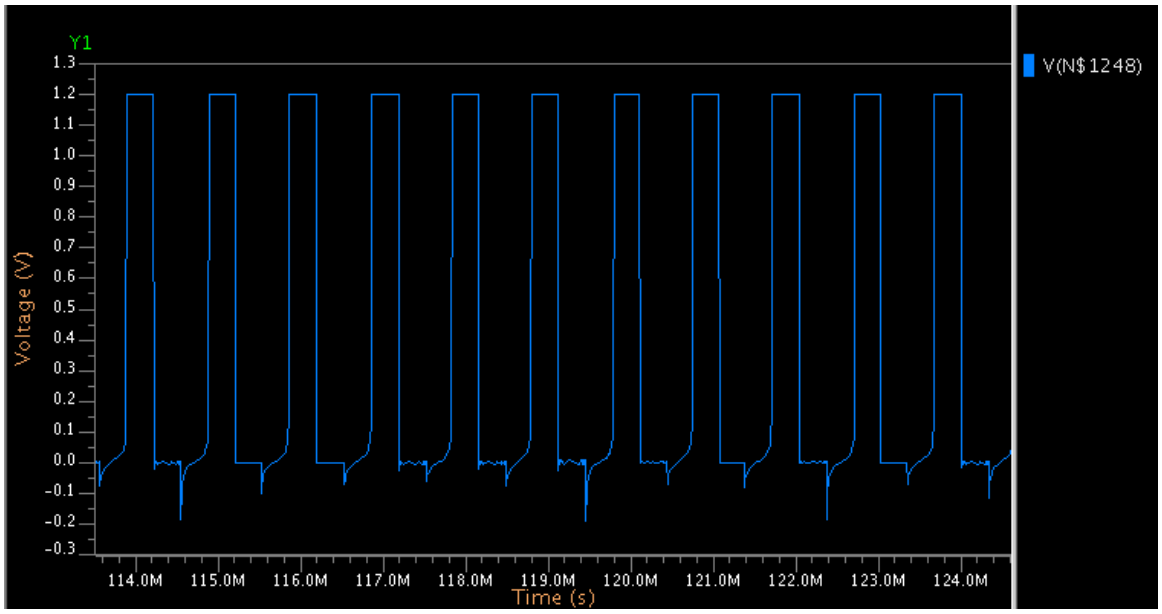
When Ptrig is precharged to VDD and Ntrig is predischarged to ground, the thyristor is turned off. Without loss of generality, Ptrig is assumed as the triggering node. Until Ptrig is discharged down to VDD - VT, M1 conducts at most the subthreshold current. Once MI is turned on, MI charges Ntrig and M2 discharges Ptrig in turn. The positive feedback mechanism in this turn-on operation provides a quick flipping of the state and reduces the dynamic power consumption. Note that no current flows directly from VDD to ground. Since there are no stacked structures which require more voltage margin, this CMOS thyristor can operate with a low supply voltage. This allows the low voltage operation of the delay element.

A delay element can be built with this CMOS thyristor and a control current source for triggering the thyristor as shown in the figure below.



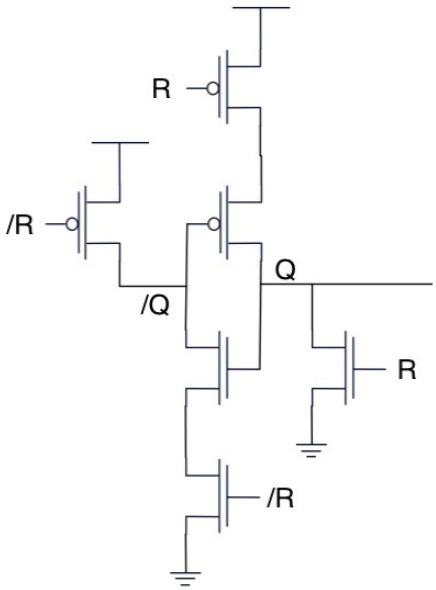
Shown below is a ring oscillator built by using three such thyristors. We obtained a output with frequency 1.02 kHz. The total power consumption was 592.6pW which is lesser than the previous two oscillator designs.





5. CMOS Tyristor based Inverter With Additional Footer Transistors

To decrease the power consumption further we can add two more transistors to limit the leakage current. The design is shown in the figure below.



The power consumed in this circuit was found to be 306 pW.

6. Comparison

The table below gives the values of various parameters for the four above mentioned oscillators after being adjusted for an output with a frequency of 1 kHz at an operating voltage of 1.2 V. Optimum value of power consumption for each configuration is determined by scaling the transistors (exception is the minimum sized Inverter Chain) and changing the number of inverters.

	No. Of Inverters	W		L		Power (nW)
SVT Inverter Chain	601	1.4um		35um		716 nW
Current Starved SVT V_b=0.2V	3	1.4um		9um (inverting transistors)	0.35um (starving transistors)	2.9 nW
CMOS Thyristor	3	1.4um		1.5um (inverting transistors)	1.3um (triggering transistors)	0.59 nW
CMOS Thyristor Footer	3	1.4um (inverting transistors)	2.8um (footer transistors)	0.35um		0.3 nW

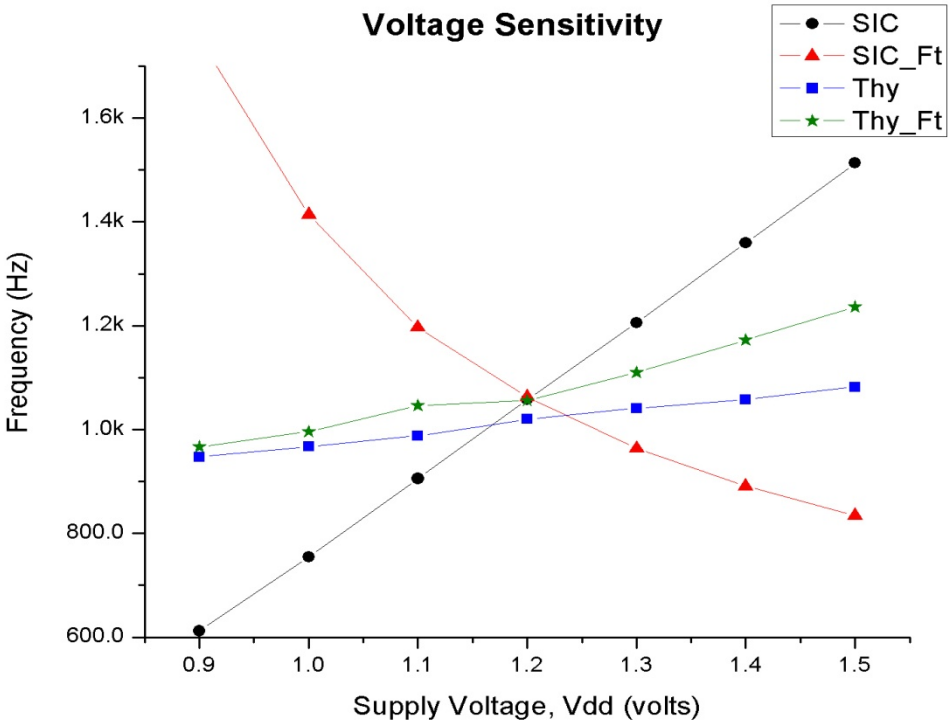
Table 2.1 Optimised Table for Minimum Power Consumption by diff. Topologies for 100 kHz at 1.2 volts.

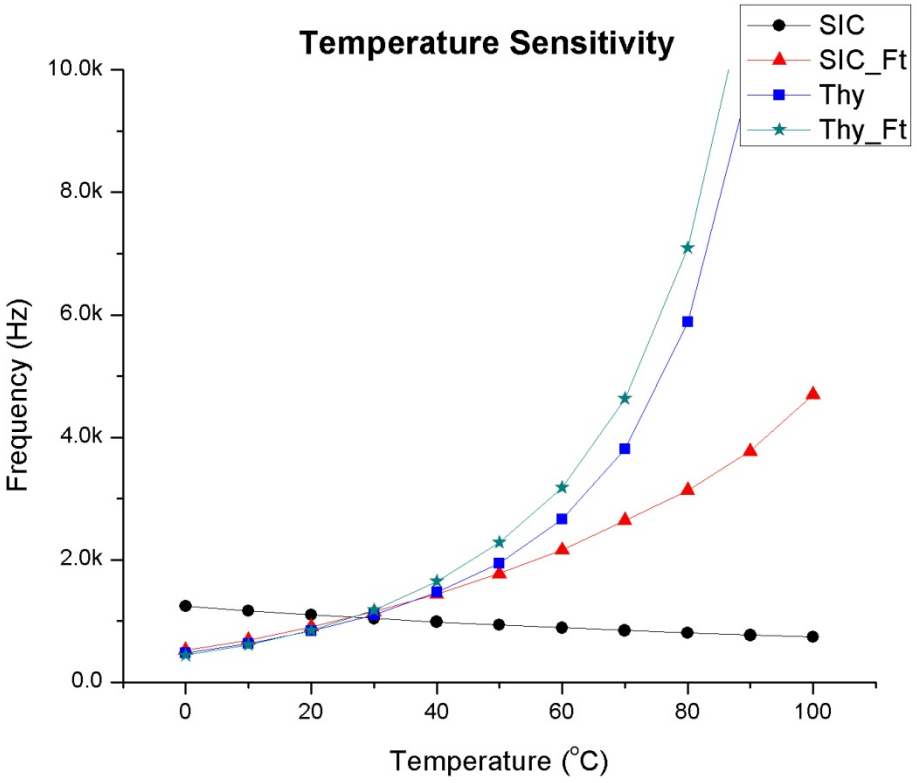
The most important point to note in the above figures is the decrease in power consumption.

Variation of frequency with supply voltage for various configurations has been determined to study the effect of voltage variations over the oscillator. It clearly shows that CMOS Thyristor & Thyristor with Footer are least sensitive to the variations in the supply voltage.

Variation of frequency with temperature is also shown below.

Hence, it is evident that CMOS Thyristor and Thyristor with footer are the best configurations for low power applications but they suffer from high temperature sensitivity. Hence, temperature compensation circuits should be used them.


Voltage Sensitivity
SIC
SIC_Ft
Thy
Thy_Ft
Frequency (Hz)
1.6k
1.4k
1.2k
1.0k
800.0
600.0
0.9
1.0
1.1
1.2
1.3
1.4
1.5
Supply Voltage, Vdd (volts)


Temperature Sensitivity
SIC
SIC_Ft
Thy
Thy_Ft
Frequency (Hz)
10.0k
8.0k
6.0k
4.0k
2.0k
0.0
0
20
40
60
80
100
Temperature (°C)